128 × 8-bit EEPROM with I²C-bus interface PCF8581/PCF8581C

GENERAL DESCRIPTION

The PCF8581 and PCF8581C are low-power CMOS EEPROMs with standard and wide operating voltage:
4.5 to 5.5 V (PCF8581); 2.5 to 6.0 V (PCF8581C).

In the following text, the generic term "PCF8581" is used to refer to both types in all packages except where specified.

The PCF8581 is organized as 128 words by 8-bits.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. All bytes can be read in a single operation. Up to eight bytes can be written in one operation, reducing the total write time per byte. Three address pins A0, A1 and A2 are used to define the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage: 4.5 to 5.5 V (PCF8581); 2.5 to 6.0 V (PCF8581C)
- Integrated voltage multiplier and timer for writing (no external components required)
- Automatic erase before write
- Low standby current max. 10 μA
- Eight-byte page write mode
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Designed for 10 000 write cycles per byte minimum
- 10 years minimum non-volatile data retention
- Infinite number of read cycles
- Pin and address compatibility to PCF8570, PCF8571 and PCF8582

PACKAGE OUTLINES

PCF8581P/PCF8581CP: 8-lead DIL; plastic (SOT97).
PCF8581T/PCF8581CT: 8-lead mini-pack (SO-8L; SOT176C).

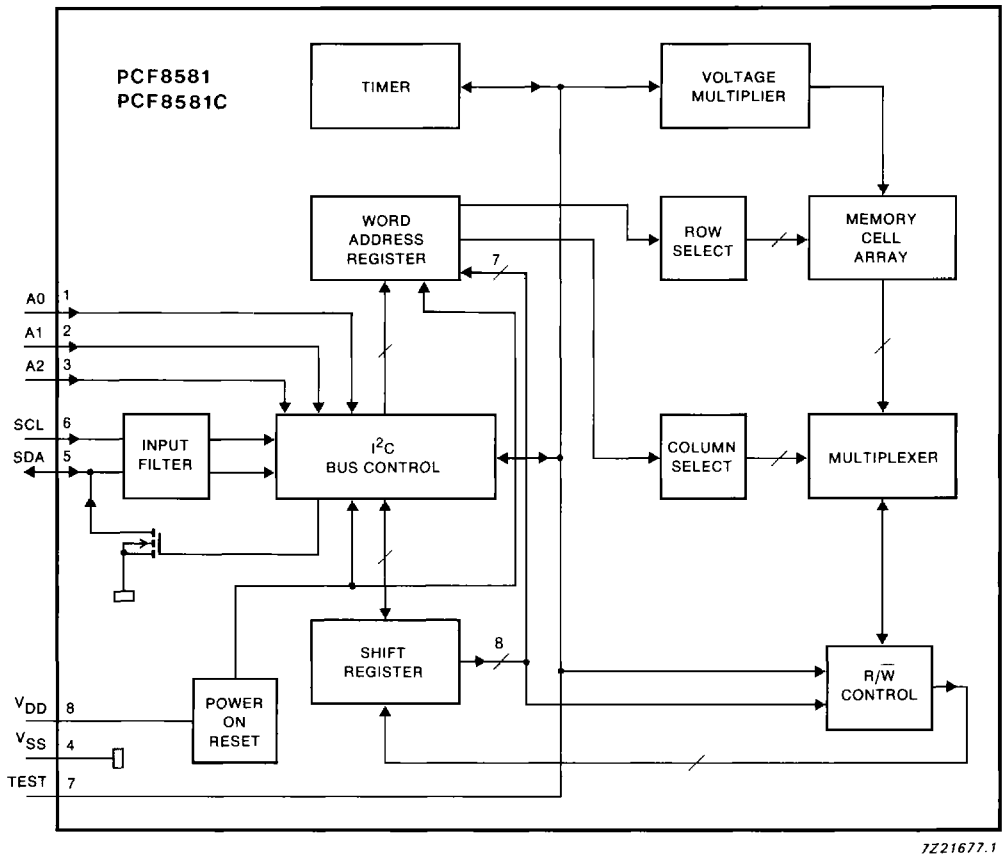


Fig.1 Block diagram.

PINNING

1	A0	hardware address inputs	
2	A1		
3	A2		
4	V_{SS}	negative supply	
5	SDA	serial data input/output	I²C-bus
6	SCL	serial clock input	
7	TEST	test output can be connected to V_{SS}, V_{DD} or left open-circuit	
8	V_{DD}	positive supply	

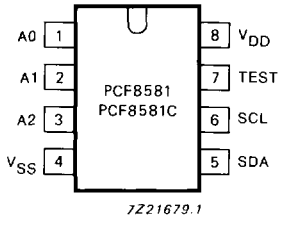


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

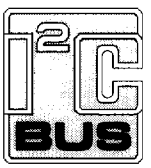
parameter	symbol	min.	max.	unit
Supply voltage range (pin 8)	V_{DD}	−0.3	7.0	V
Voltage range on any input*	V_I	−0.8	V_{DD} + 0.8	V
DC input current (any input)	$\pm I_I$	–	10	mA
DC output current (any output)	$\pm I_O$	–	10	mA
Total power dissipation	P_{tot}	–	150	mW
Power dissipation per output	P	–	50	mW
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C

* Measured via a 500 Ω resistor.

CHARACTERISTICS

V_{DD} = 2.5 to 6 V (PCF8581C) 4.5 to 5.5 V (PCF8581); V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range						
PCF8581A		V_{DD}	2.5	–	6.0	V
PCF8581		V_{DD}	4.5	–	5.5	V
Supply current						
standby	f_{SCL} = 0 Hz	I_{DD}	–	–	10	μA
operating	f_{SCL} = 100 kHz	I_{DD}	–	–	400	μA
during write	see bus protocol	I_{DD}	–	–	1000	μA
Inputs						
A0, A1, A2, SCL, SDA						
Input voltage LOW		V_{IL}	–	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	–	V
Input leakage current	pin at V_{SS} or V_{DD}	I_{LI}	–	–	1	μA
Input capacitance	pin at V_{SS}	C_I	–	–	7	pF
Outputs						
SDA						
Output current LOW	pin at 0.4 V	I_{OL}	3	–	–	mA
TEST						
Output leakage current	pin at V_{SS} or V_{DD}	I_{LO}	–	–	1	μA
Erase/write data						
Write time		t_{WR}	6	–	12	ms
Data retention time		t_{RET}	10	–	–	years



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for two-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

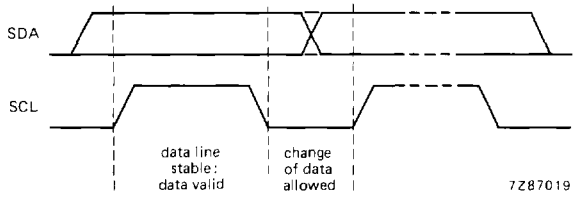


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

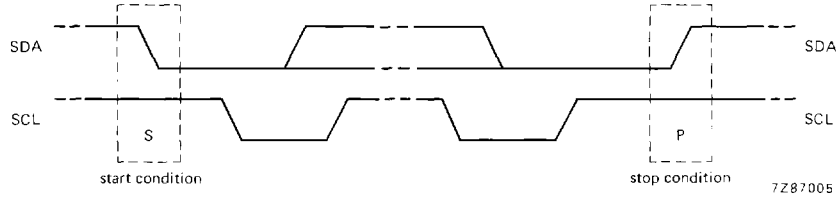


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

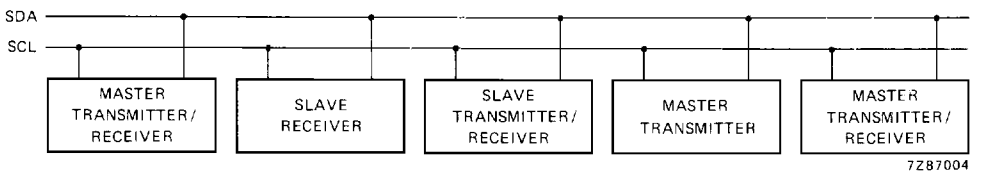


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eigth bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

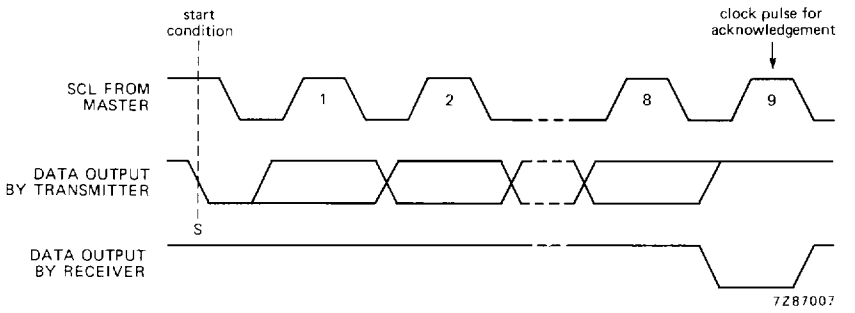


Fig. 6 Acknowledgement on the I²C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

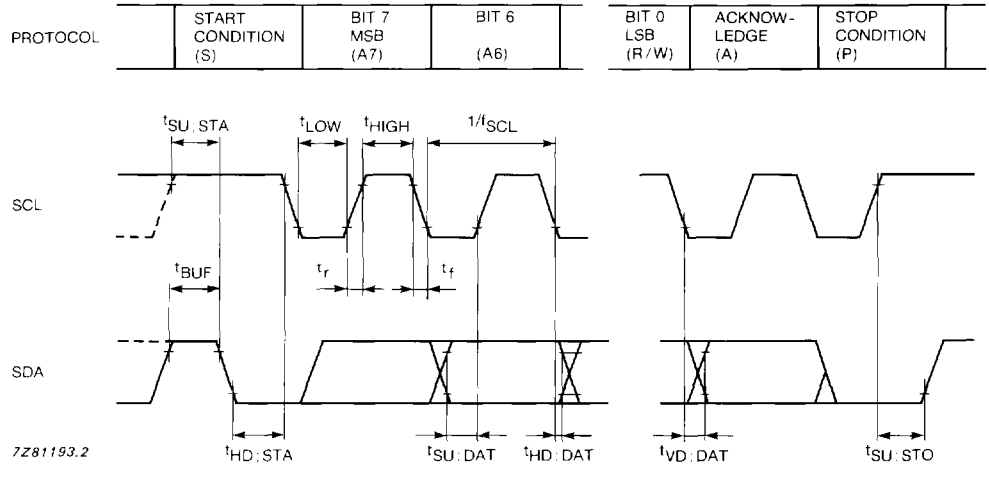


Fig. 7 I²C-bus timing diagram.

Bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C-bus configuration for PCF8581 WRITE cycle is shown in Fig. 8 and READ cycle in Figs 10 and 11.

Writing

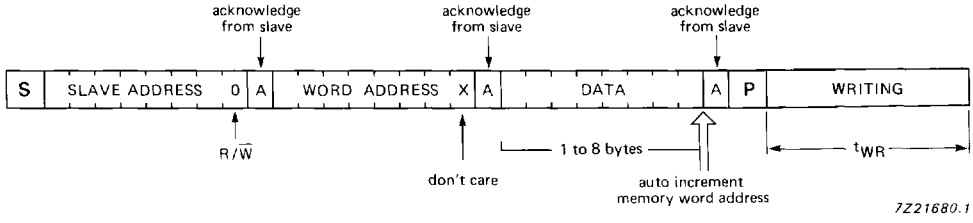


Fig. 8 Master transmits to slave receiver (WRITE mode).

After the word address, one to eight data bytes can be sent. The address is automatically incremented, but the four highest address bits (row) are internally latched. Therefore all bytes are written in the same row.

An example of writing eight bytes with word address X0000000 and six bytes with word address X0010101 is shown in Fig. 9. Where X = don't care.

word address	row	bytes							
X0000000	0	1 →	2 →	3 →	4 →	5 →	6 →	7 →	8 →
X0000001	1								
X0010101	2	4 →	5 →	6			1 →	2 →	3 → →
X0011101	3								
	•								
	•								
column		0	1	2	3	4	5	6	7

Fig. 9 Writing eight and six bytes with different word addresses.

To transmit eight bytes in sequential order, begin with the lowest address bits 000. The data is written after a stop is detected. The data is only written if complete bytes have been received and acknowledged. Writing takes a time t_{WR} (6 to 12 ms) during which the device will not respond to its slave address. Note that to write the next row, a new write operation is required (start, slave address, row address, data, stop).

Reading

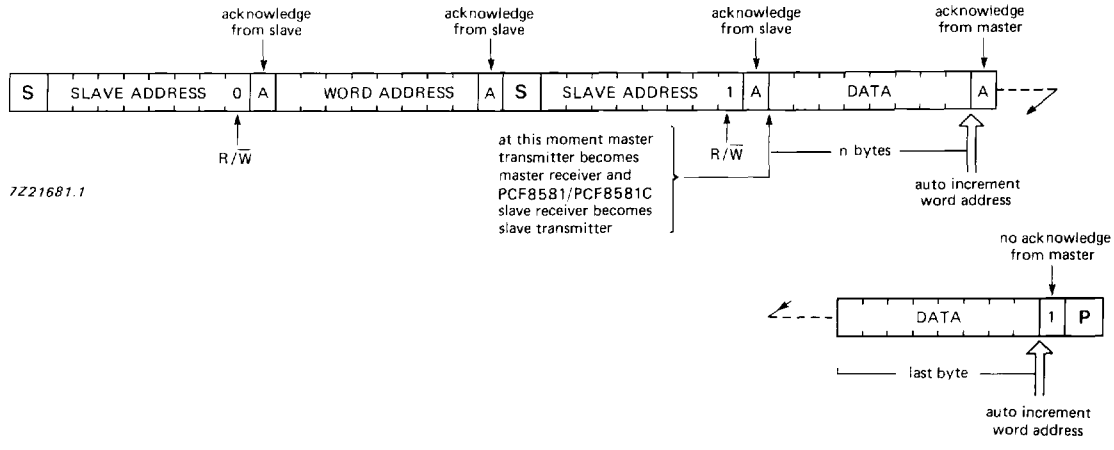


Fig. 10 Master reads after setting word address (WRITE word address; READ data).

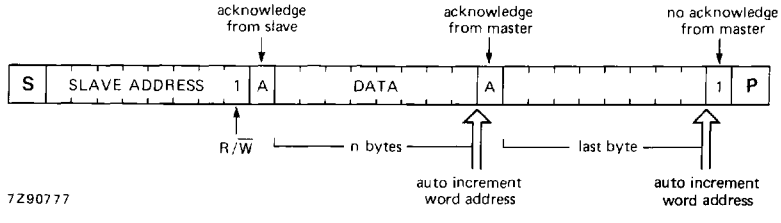


Fig. 11 Master reads slave immediately after first byte (READ mode).

An unlimited number of data bytes can be read in one operation. The address is automatically incremented. If a read without setting the word address is performed after a write operation, the address pointer may point at a byte in the row after the previously written row. This occurs if, during writing, the three lowest address bits (column) rolled over.

APPLICATION INFORMATION

The PCF8581 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 12).

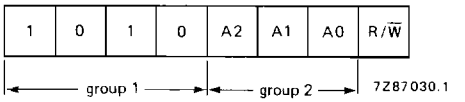


Fig. 12 PCF8581 address.

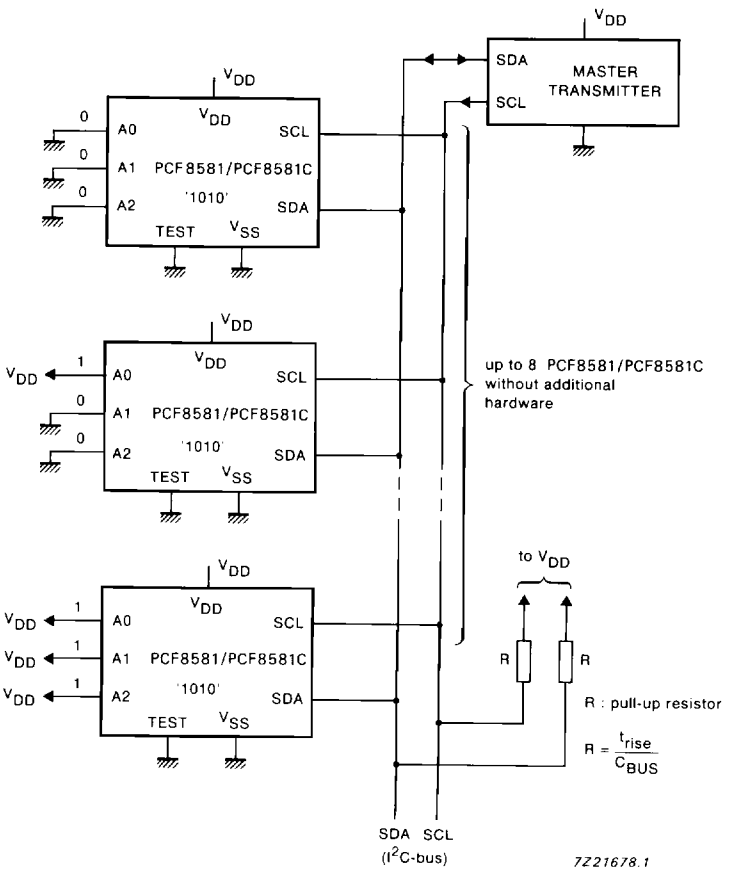


Fig. 13 Application diagram.

Note

A0, A1 and A2 inputs must be connected to V_{DD} or V_{SS} but not left open-circuit.