

Transistors

4V Drive Nch+Pch MOS FET

SP8M2

●Structure

Silicon N-channel MOS FET /
Silicon P-channel MOS FET

●Features

- 1) Low on-resistance.
- 2) Built-in G-S protection diode.
- 3) Small surface mount package (SOP8).

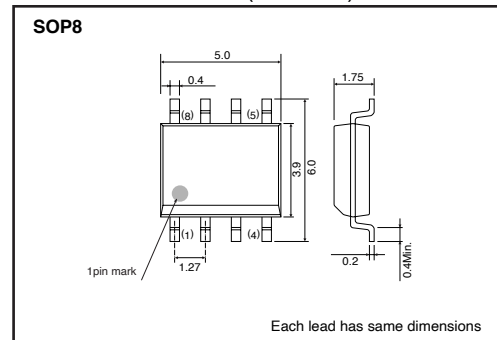
●Applications

Switching

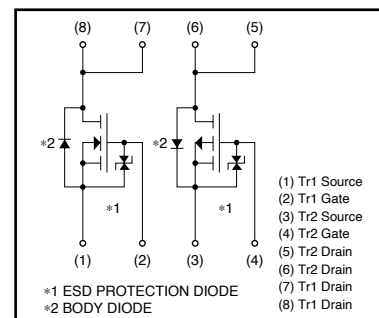
●Package specifications

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
SP8M2		○

●External dimensions (Unit : mm)



●Inner circuit



●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit
		Tr1 : N-ch	Tr2 : P-ch	
Drain-source voltage	V_{DSS}	30	-30	V
Gate-source voltage	V_{GSS}	20	-20	V
Drain current	Continuous	I_D	± 3.5	A
	Pulsed	I_{DP}^{*1}	± 14	A
Source current (Body diode)	Continuous	I_S	1.6	A
	Pulsed	I_{SP}^{*1}	14	A
Total power dissipation	P_D^{*2}	2.0		W / TOTAL
Channel temperature	Tch	150		°C
Storage temperature	Tstg	-55 to +150		°C

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$
*2 Mounted on a ceramic board.

Transistors

N-ch

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	10	μA	$V_{GS}=20V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR) DSS}$	30	–	–	V	$I_D=1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	–	–	1	μA	$V_{DS}=30V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	1.0	–	2.5	V	$V_{DS}=10V, I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	–	59	83	$m\Omega$	$I_D=3.5A, V_{GS}=10V$
		–	93	130	$m\Omega$	$I_D=3.5A, V_{GS}=4.5V$
		–	107	150	$m\Omega$	$I_D=3.5A, V_{GS}=4V$
Forward transfer admittance	$ Y_{fs} $ *	2.0	–	–	S	$V_{DS}=10V, I_D=3.5A$
Input capacitance	C_{iss}	–	140	–	pF	$V_{DS}=10V$
Output capacitance	C_{oss}	–	45	–	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	–	30	–	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	–	6	–	ns	$V_{DD} \doteq 15V$
Rise time	t_r *	–	6	–	ns	$I_D=1.75A$
Turn-off delay time	$t_{d(off)}$ *	–	17	–	ns	$V_{GS}=10V$
Fall time	t_f *	–	4	–	ns	$R_L=8.57\Omega$
Total gate charge	Q_g *	–	2.5	3.5	nC	$V_{DD} \doteq 15V, V_{GS}=5V$
Gate-source charge	Q_{gs} *	–	0.8	–	nC	$I_D=3.5A$
Gate-drain charge	Q_{gd} *	–	0.8	–	nC	$R_L=4.29\Omega, R_G=10\Omega$

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	–	–	1.2	V	$I_S=6.4A, V_{GS}=0V$

*Pulsed

Transistors

P-ch

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	–10	μA	$V_{GS} = -20V, V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR) DSS}$	–30	–	–	V	$I_D = -1mA, V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}	–	–	–1	μA	$V_{DS} = -30V, V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	–1.0	–	–2.5	V	$V_{DS} = -10V, I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	–	65	90	m Ω	$I_D = -3.5A, V_{GS} = -10V$
		–	100	140	m Ω	$I_D = -1.75A, V_{GS} = -4.5V$
		–	120	165	m Ω	$I_D = -1.75A, V_{GS} = -4V$
Forward transfer admittance	$ Y_{fs} $ *	1.8	–	–	S	$V_{DS} = -10V, I_D = -1.75A$
Input capacitance	C_{iss}	–	490	–	pF	$V_{DS} = -10V$
Output capacitance	C_{oss}	–	110	–	pF	$V_{GS} = 0V$
Reverse transfer capacitance	C_{rss}	–	75	–	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$ *	–	10	–	ns	$V_{DD} = -15V$
Rise time	t_r *	–	15	–	ns	$I_D = -1.75A$
Turn-off delay time	$t_{d(off)}$ *	–	35	–	ns	$V_{GS} = -10V$
Fall time	t_f *	–	10	–	ns	$R_L = 8.57\Omega$
Total gate charge	Q_g *	–	5.5	7.7	nC	$V_{DD} = -15V, V_{GS} = -5V$
Gate-source charge	Q_{gs} *	–	1.5	–	nC	$I_D = -3.5A$
Gate-drain charge	Q_{gd} *	–	2.0	–	nC	$R_L = 4.29\Omega, R_G = 10\Omega$

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	–	–	–1.2	V	$I_S = -1.6A, V_{GS} = 0V$

*Pulsed

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