

DATA SHEET



SAA55xx

TV microcontrollers with Closed
Captioning (CC) and On-Screen
Display (OSD)

Preliminary specification
File under Integrated Circuits, IC02

1999 Aug 02

TV microcontrollers with Closed Captioning (CC) and On-Screen Display (OSD)

SAA55xx

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TV microcontrollers with Closed Captioning (CC) and On-Screen Display (OSD)

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1 FEATURES

- Single-chip microcontroller with integrated On-Screen Display (OSD)
- One Time Programmable (OTP) memory for both Program ROM and character sets
- Single power supply: 3.0 to 3.6 V
- 5 V tolerant digital inputs and I/O
- 29 I/O port via individual addressable controls
- Programmable I/O for push-pull, open-drain and quasi-bidirectional
- Two port lines with 8 mA sink (at <math><0.4\text{ V}</math>) capability, for direct drive of Light Emitting Diode (LED)
- Single crystal oscillator for microcontroller, OSD and data capture
- Power reduction modes: Standby, Idle and Power-down
- Byte level I²C-bus up to 200 kHz with dual port I/O (Slave mode up to 400 kHz)
- 32 Dynamically Redefinable Characters for OSDs
- Special graphic characters allowing four colours per character
- Selectable character height 9, 10, 13 and 16 TV lines
- Pin compatibility throughout family
- Operating temperature: -20 to +70°C



2 GENERAL DESCRIPTION

The SAA55xx OSD only family of devices are a derivative of the Philips industry standard 80C51 microcontroller and are intended for use as the central control mechanism in a television receiver. They provide control functions for the television system, On-Screen Display (OSD) and some versions include an integrated data capture function.

The main differences between the OSD only family and the SAA55xx Text/CC family of baseline devices are:

- Program ROM size: 16 to 64-kbyte
- Display DRAM size: 1.25-kbyte (1 page Text OSD or CC/OSD)
- Auxiliary DRAM size: 0.75-kbyte
- No teletext data capture (Closed Caption only)
- Additional power saving mode (Standby).

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3 QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------------|---|------|------|------|--------------|
| Supply | | | | | |
| V_{DDX} | any supply voltage (V_{DD} to V_{SS}) | 3.0 | 3.3 | 3.6 | V |
| I_{DDP} | periphery supply current; note 1 | 1 | – | – | mA |
| I_{DDC} | core supply current | – | 12 | 18 | mA |
| $I_{DDC(id)}$ | Idle mode core supply current | – | 383 | 600 | μ A |
| $I_{DDC(pd)}$ | Power-down mode core supply current | – | 666 | 900 | μ A |
| $I_{DDC(stb)}$ | Standby mode core supply current | – | 5.1 | 9 | mA |
| I_{DDA} | analog supply current | – | 45 | 48 | mA |
| $I_{DDA(id)}$ | Idle mode analog supply current | – | 444 | 700 | μ A |
| $I_{DDA(pd)}$ | Power-down mode analog supply current | – | 433 | 700 | μ A |
| $I_{DDA(stb)}$ | Standby mode core supply current | – | 809 | 950 | μ A |
| f_{xtal} | Fundamental mode nominal frequency | – | 12 | – | MHz |
| T_{amb} | operating ambient temperature | –20 | – | +70 | $^{\circ}$ C |
| T_{stg} | storage temperature | –55 | – | +125 | $^{\circ}$ C |

Note

- Peripheral supply current is dependent on external components and voltage levels on I/Os.

4 ORDERING INFORMATION

| TYPE NUMBER ⁽¹⁾ | PACKAGE ⁽²⁾ | | | ROM | RAM | CC | OSD |
|----------------------------|------------------------|---|----------|----------|----------|-----|----------|
| | NAME | DESCRIPTION | VERSION | | | | |
| SAA5500PS/nnnn | SDIP52 | plastic shrink dual in-line package; 52 leads (600 mil) | SOT247-1 | 16-kbyte | 256-byte | no | Standard |
| SAA5501PS/nnnn | | | | 32-kbyte | 512-byte | no | Standard |
| SAA5540PS/nnnn | | | | 16-kbyte | 256-byte | yes | Enhanced |
| SAA5541PS/nnnn | | | | 32-kbyte | 512-byte | yes | Enhanced |
| SAA5502PS/nnnn | | | | 48-kbyte | 256-byte | no | Standard |
| SAA5503PS/nnnn | | | | 64-kbyte | 512-byte | no | Standard |
| SAA5542PS/nnnn | | | | 48-kbyte | 750-byte | yes | Enhanced |
| SAA5543PS/nnnn | | | | 64-kbyte | 1-kbyte | yes | Enhanced |
| SAA5547PS/nnnn | | | | 24-kbyte | 750-byte | yes | Enhanced |

Notes

- 'nnnn' is a four digit number uniquely referencing the microcontroller program mask.
- For details of the LQFP100 package, please contact your local regional sales office for availability.

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5 BLOCK DIAGRAM

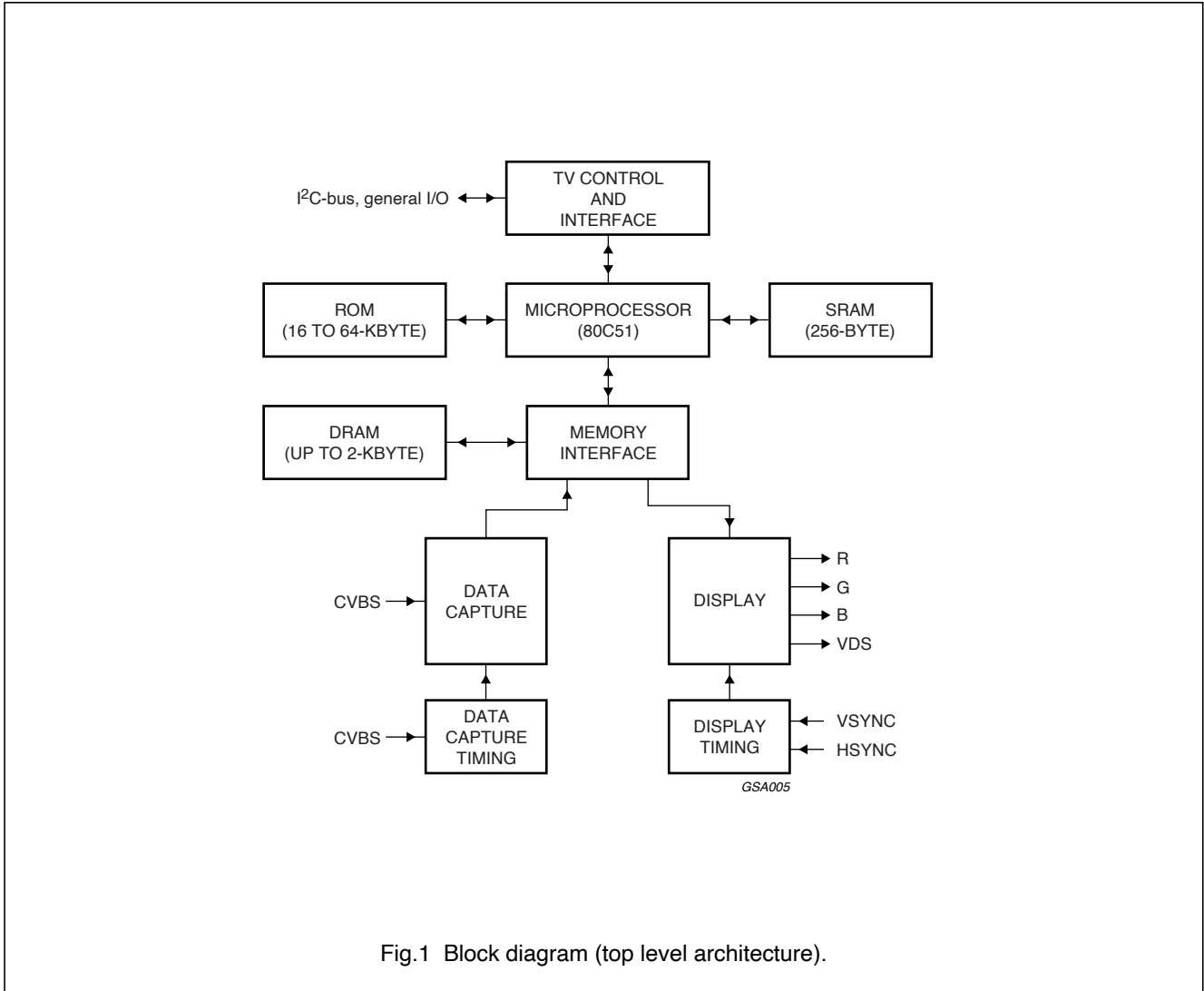


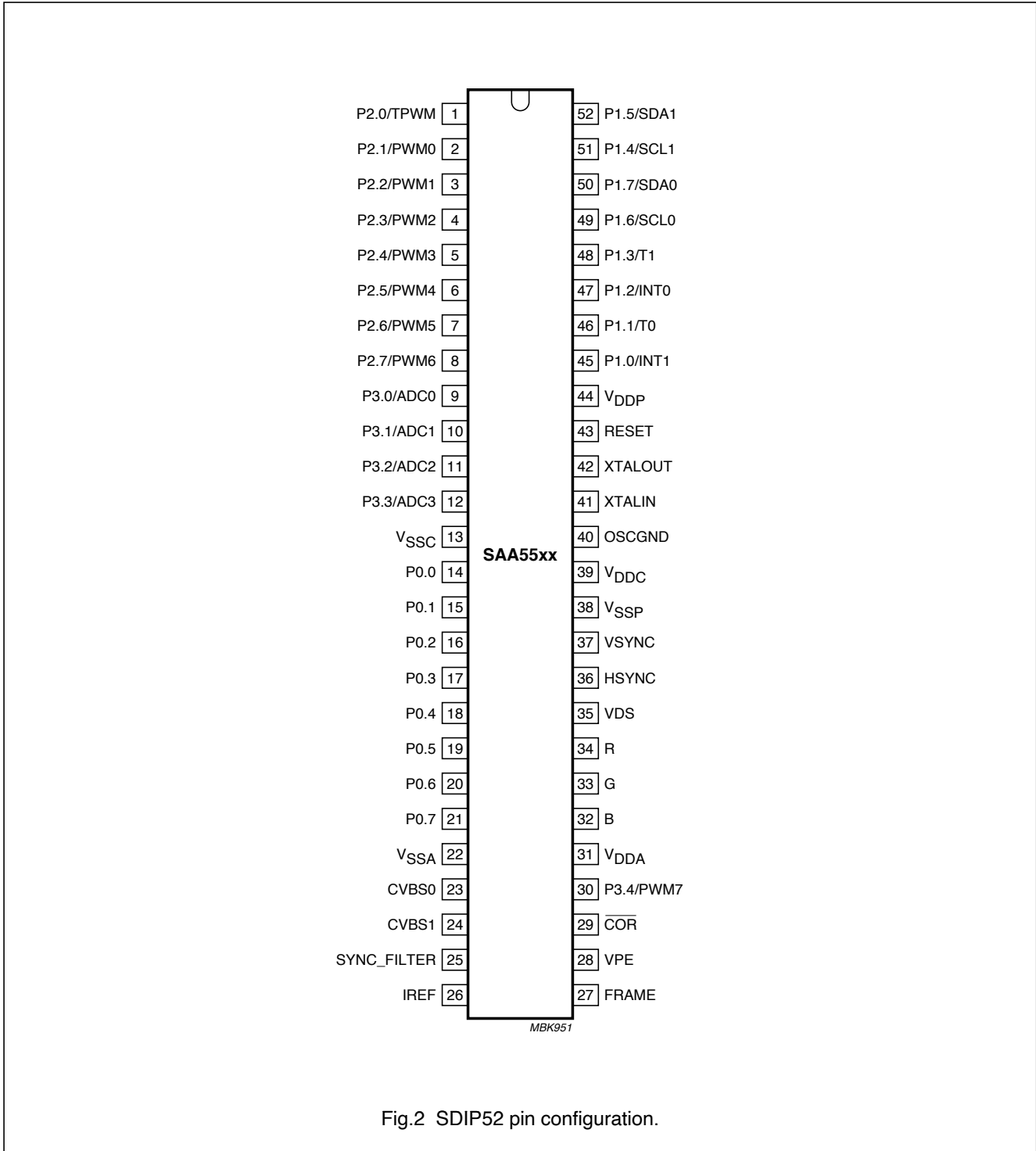
Fig.1 Block diagram (top level architecture).

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6 PINNING INFORMATION

6.1 Pinning



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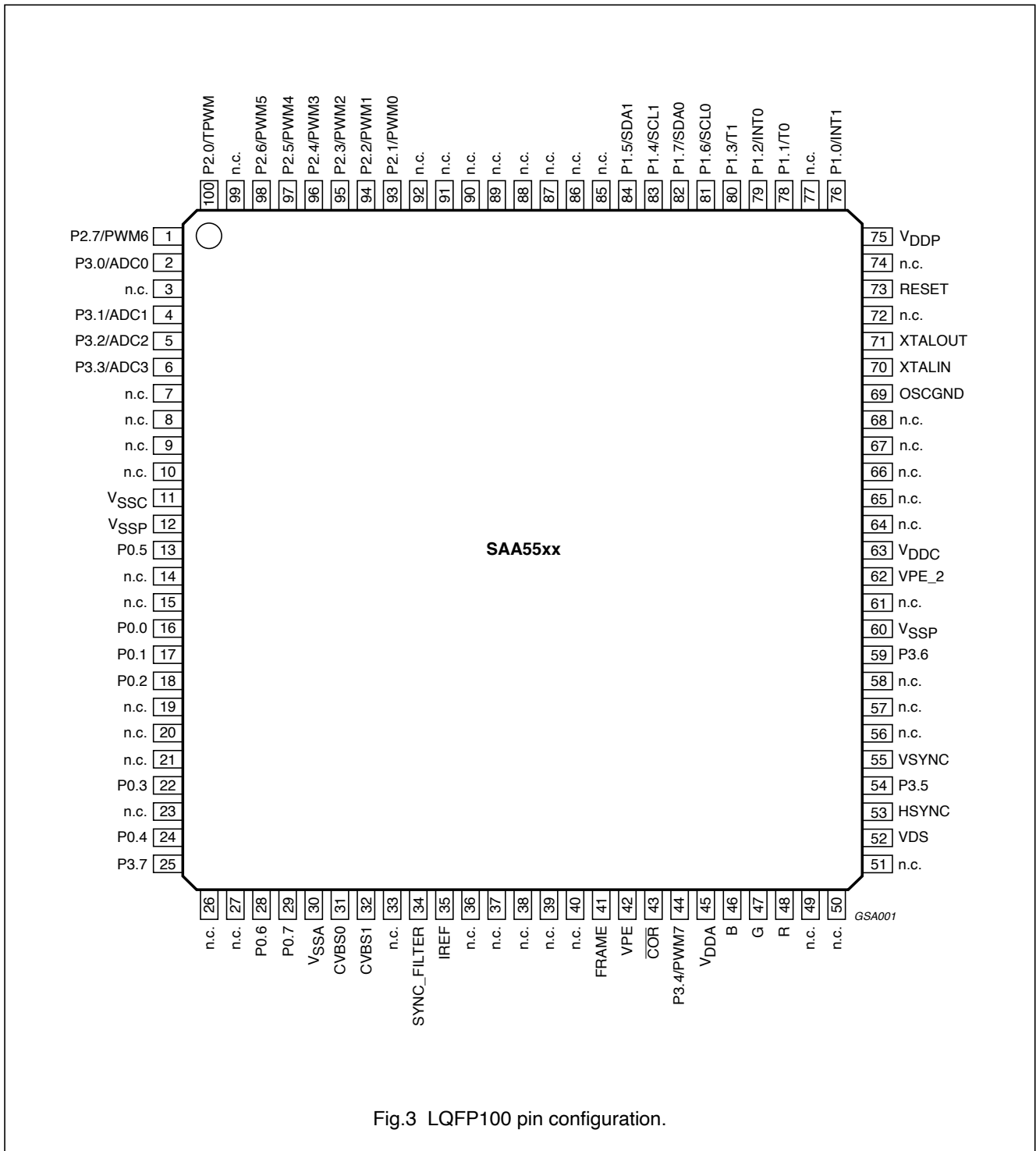


Fig.3 LQFP100 pin configuration.

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6.2 Pin description

Table 1 SDIP52 and LQFP100 packages

| SYMBOL | PIN | | TYPE | DESCRIPTION |
|------------------|--------|---------|------|--|
| | SDIP52 | LQFP100 | | |
| P2.0/TPWM | 1 | 100 | I/O | Port 2. 8-bit programmable bidirectional port with alternative functions. P2.0/TPWM is the output for the 14-bit high precision PWM. P2.1/PWM0 to P2.7/PWM6 are the outputs for the 6-bit PWMs 0 to 6. |
| P2.1/PWM0 | 2 | 93 | I/O | |
| P2.2/PWM1 | 3 | 94 | I/O | |
| P2.3/PWM2 | 4 | 95 | I/O | |
| P2.4/PWM3 | 5 | 96 | I/O | |
| P2.5/PWM4 | 6 | 97 | I/O | |
| P2.6/PWM5 | 7 | 98 | I/O | |
| P2.7/PWM6 | 8 | 1 | I/O | |
| P3.0/ADC0 | 9 | 2 | I/O | Port 3. 8-bit programmable bidirectional port with alternative functions. P3.0/ADC0 to P3.3/ADC3 are the inputs for the software ADC facility. P3.4/PWM7 is the output for the 6-bit PWM7. P3.5 to P3.7 have no alternative functions and are only available with the LQFP100 package. |
| P3.1/ADC1 | 10 | 4 | I/O | |
| P3.2/ADC2 | 11 | 5 | I/O | |
| P3.3/ADC3 | 12 | 6 | I/O | |
| P3.4/PWM7 | 30 | 44 | I/O | |
| P3.5 | – | 54 | I/O | |
| P3.6 | – | 59 | I/O | |
| P3.7 | – | 25 | I/O | |
| V _{SSC} | 13 | 11 | – | core ground |
| P0.0 | 14 | 16 | I/O | Port 0. 8-bit programmable bidirectional port. P0.5 and P0.6 have 8 mA current sinking capability for direct drive of LEDs. |
| P0.1 | 15 | 17 | I/O | |
| P0.2 | 16 | 18 | I/O | |
| P0.3 | 17 | 22 | I/O | |
| P0.4 | 18 | 24 | I/O | |
| P0.5 | 19 | 13 | I/O | |
| P0.6 | 20 | 28 | I/O | |
| P0.7 | 21 | 29 | I/O | |
| V _{SSA} | 22 | 30 | – | analog ground |
| CVBS0 | 23 | 31 | I | Composite Video Baseband Signal (CVBS) input. A positive-going 1 V (peak-to-peak) input is required. |
| CVBS1 | 24 | 32 | I | Connected via a 100 nF capacitor. |
| SYNC_FILTER | 25 | 34 | I | CVBS sync filter input. This pin should be connected to V _{SSA} via a 100 nF capacitor. |
| IREF | 26 | 35 | I | Reference current input for analog circuits, connected to V _{SSA} via a 24 K Ω resistor. |
| FRAME | 27 | 41 | O | De-interlace output synchronised with the VSYNC pulse to produce a non-interlaced display by adjustment of the vertical deflection circuits. |
| VPE | 28 | 42 | I | OTP programming voltage |

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| SYMBOL | PIN | | TYPE | DESCRIPTION |
|------------------|--------|--|------|---|
| | SDIP52 | LQFP100 | | |
| COR | 29 | 43 | O | Open-drain, active LOW output which allows selective contrast reduction of the TV picture to enhance a mixed mode display. |
| V _{DDA} | 31 | 45 | – | +3.3 V analog power supply |
| B | 32 | 46 | O | Pixel rate output of the BLUE colour information. |
| G | 33 | 47 | O | Pixel rate output of the GREEN colour information. |
| R | 34 | 48 | O | Pixel rate output of the RED colour information. |
| VDS | 35 | 52 | O | Video/data switch push-pull output for dot rate fast blanking. |
| HSYNC | 36 | 53 | I | Schmitt triggered input TTL version of the horizontal sync pulse. The polarity of this pulse is programmable by register bit TXT1.H POLARITY. |
| VSYNC | 37 | 55 | I | Schmitt triggered input for a TTL version of the vertical sync pulse. The polarity of this pulse is programmable by register bit TXT1.V POLARITY. |
| V _{SSP} | 38 | 12, 60 | – | periphery ground |
| V _{DDC} | 39 | 63 | – | +3.3 V core power supply |
| OSCGND | 40 | 69 | – | crystal oscillator ground |
| XTALIN | 41 | 70 | I | 12 MHz crystal oscillator input |
| XTALOUT | 42 | 71 | O | 12 MHz crystal oscillator output |
| RESET | 43 | 73 | I | If the reset input is HIGH for at least 2 machine cycles (24 oscillator periods) while the oscillator is running, the device is reset. This pin should be connected to V _{DDP} via a capacitor. |
| V _{DDP} | 44 | 75 | – | +3.3 V periphery power supply |
| P1.0/INT1 | 45 | 76 | I/O | Port 1. 8-bit programmable bidirectional port with alternative functions. P1.0/INT1 is external interrupt 1 which can be triggered on the rising and falling edge of the pulse. P1.1/T0 is the Counter/Timer 0. P1.2/INT0 is external interrupt 0. P1.3/T1 is the Counter/Timer 1. P1.6/SCL0 is the serial clock input for the I ² C-bus and P1.7/SDA0 is the serial data port for the I ² C-bus. P1.4/SCL1 is the serial clock input for the I ² C-bus and P1.5/SDA1 is the serial data port for the I ² C-bus. |
| P1.1/T0 | 46 | 78 | I/O | |
| P1.2/INT0 | 47 | 79 | I/O | |
| P1.3/T1 | 48 | 80 | I/O | |
| P1.6/SCL0 | 49 | 81 | I/O | |
| P1.7/SDA0 | 50 | 82 | I/O | |
| P1.4/SCL1 | 51 | 83 | I/O | |
| P1.5/SDA1 | 52 | 84 | I/O | |
| VPE_2 | – | 62 | I | OTP programming voltage |
| n.c. | – | 3, 7 to 10, 14, 15, 19 to 21, 23, 26, 27, 33, 36 to 40, 49 to 51, 56 to 58, 61, 64 to 68, 72, 74, 77, 85 to 92, 99 | – | not connected |

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7 MICROCONTROLLER

The functionality of the microcontroller used on this device is described here with reference to the industry standard 80C51 microcontroller. A full description of its functionality can be found in the *“Painter 1 Hardware System Specification and Tentative Device Specification (Painter1.1/1.10)”*.

7.1 Microcontroller features

- 80C51 microcontroller core standard instruction set and timing
- 1 μ s machine cycle
- Maximum 64K \times 8-bit program ROM
- 2 \times 8-bit auxiliary RAM, maximum of 1.25 kbytes required for display
- Interrupt controller for individual enable/disable with two level priority
- Two 16-bit timer/counter registers
- Watchdog Timer
- Auxiliary RAM page pointer
- 16-bit data pointer
- Standby, Idle and Power-down modes
- 29 general I/O lines
- Eight 6-bit Pulse Width Modulator (PWM) outputs for control of TV analog signals
- One 14-bit PWM for Voltage Synthesis Tuner (VST) control
- 8-bit Analog-to-Digital Converter (ADC) with four multiplexed inputs
- 2 high current outputs for directly driving LEDs
- I²C-bus byte level bus interface with dual ports.

8 MEMORY ORGANIZATION

The device has the capability of a maximum of 64-kbyte Program ROM and 2-kbyte Data RAM internally.

8.1 ROM bank switching

As the Program ROM does not exceed 64 kbytes in any of the OSD only variants, ROM bank switching is not required.

The memory and security bits are structured as shown in Fig.4.

The OSD only security bits are set as shown in Fig.5 for production programmed devices.

The OSD only security bits are set as shown in Fig.6 for production blank devices.

8.2 RAM organisation

The Internal Data RAM is organized into two areas, Data memory and Special Function Registers (SFRs).

8.3 Data memory

The Data memory is 256 \times 8-bit, and occupies the address range 00H to FFH when using indirect addressing and 00H to 7FH when using direct addressing. The SFRs occupy the address range 80H to FFH and are accessible using direct addressing only.

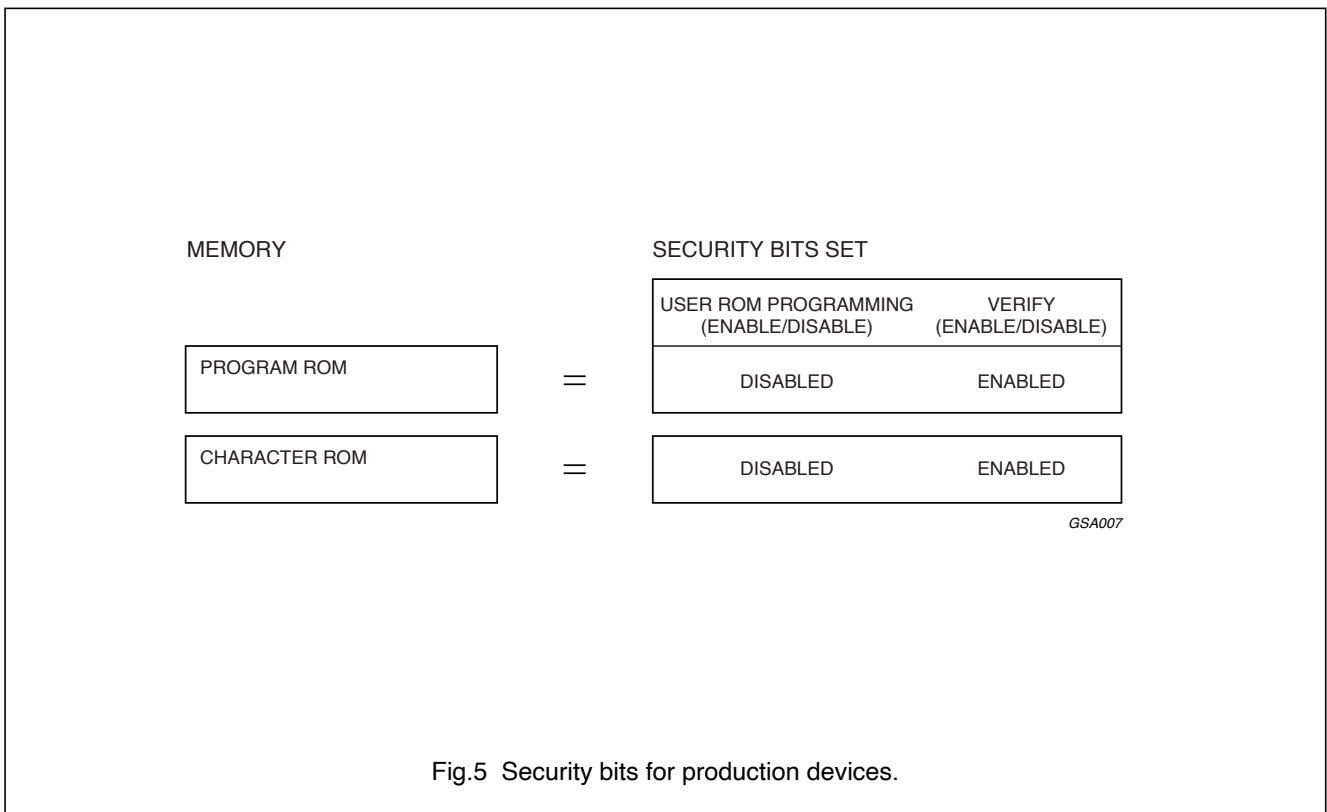
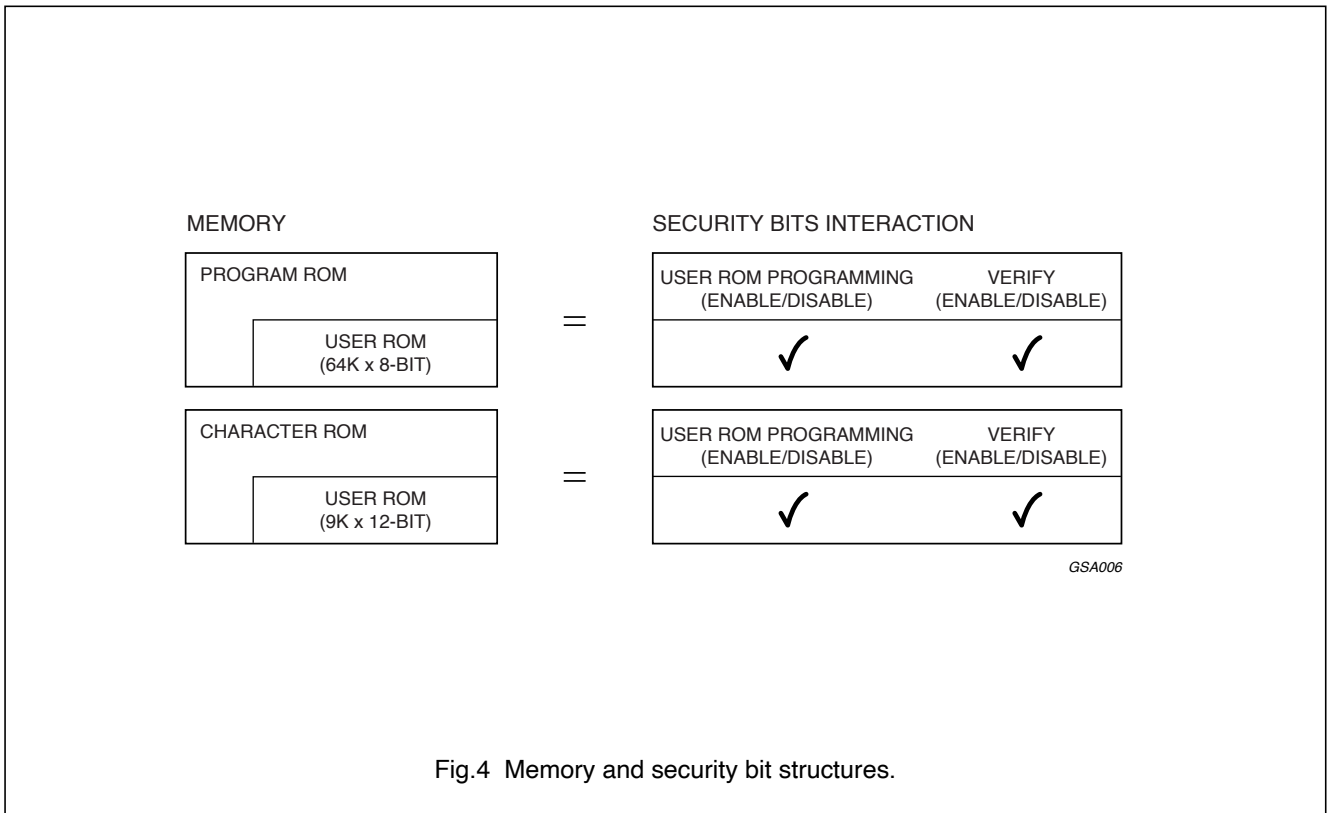
The lower 128 bytes of Data memory are mapped as shown in Fig.8.

The lowest 24 bytes are grouped into 4 banks of 8 registers, the next 16 bytes above the register banks form a block of bit addressable memory space.

The upper 128 bytes are not allocated for any special area or functions.

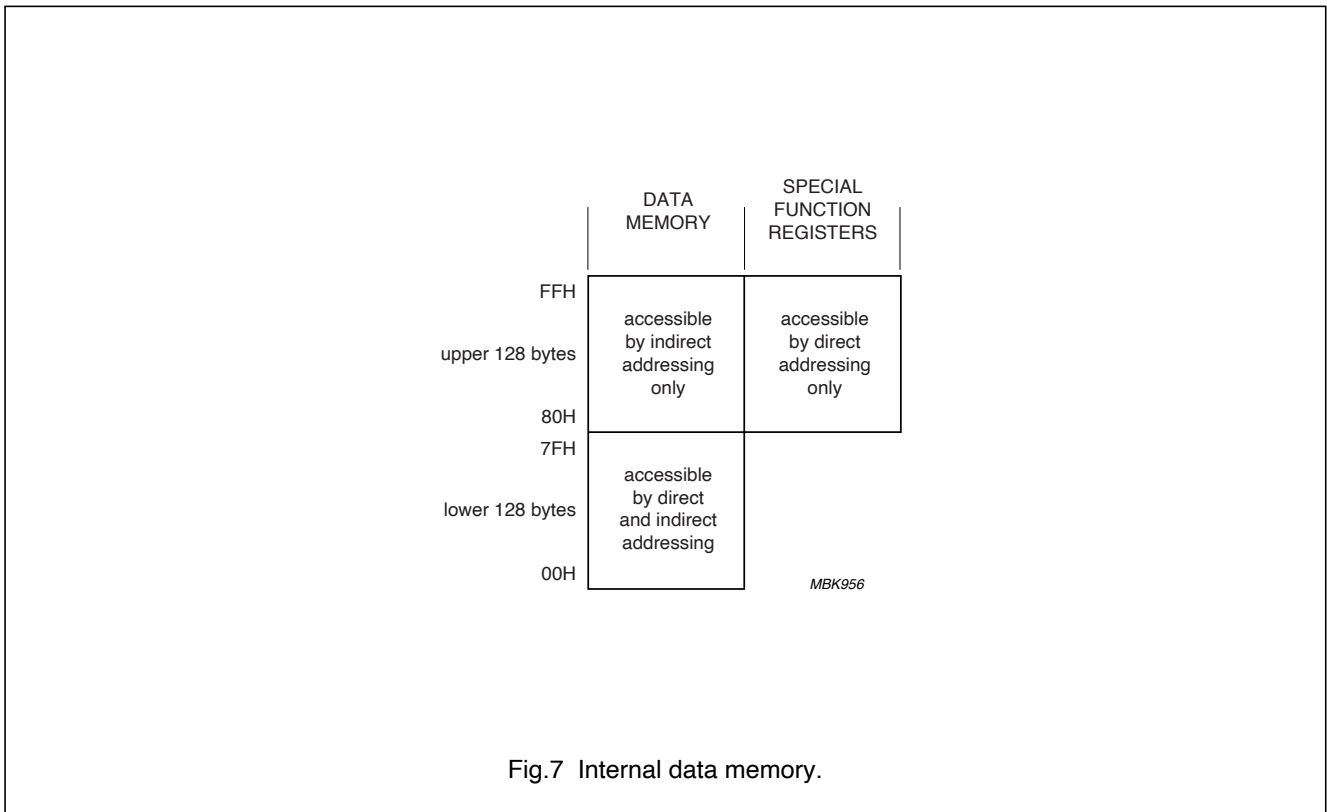
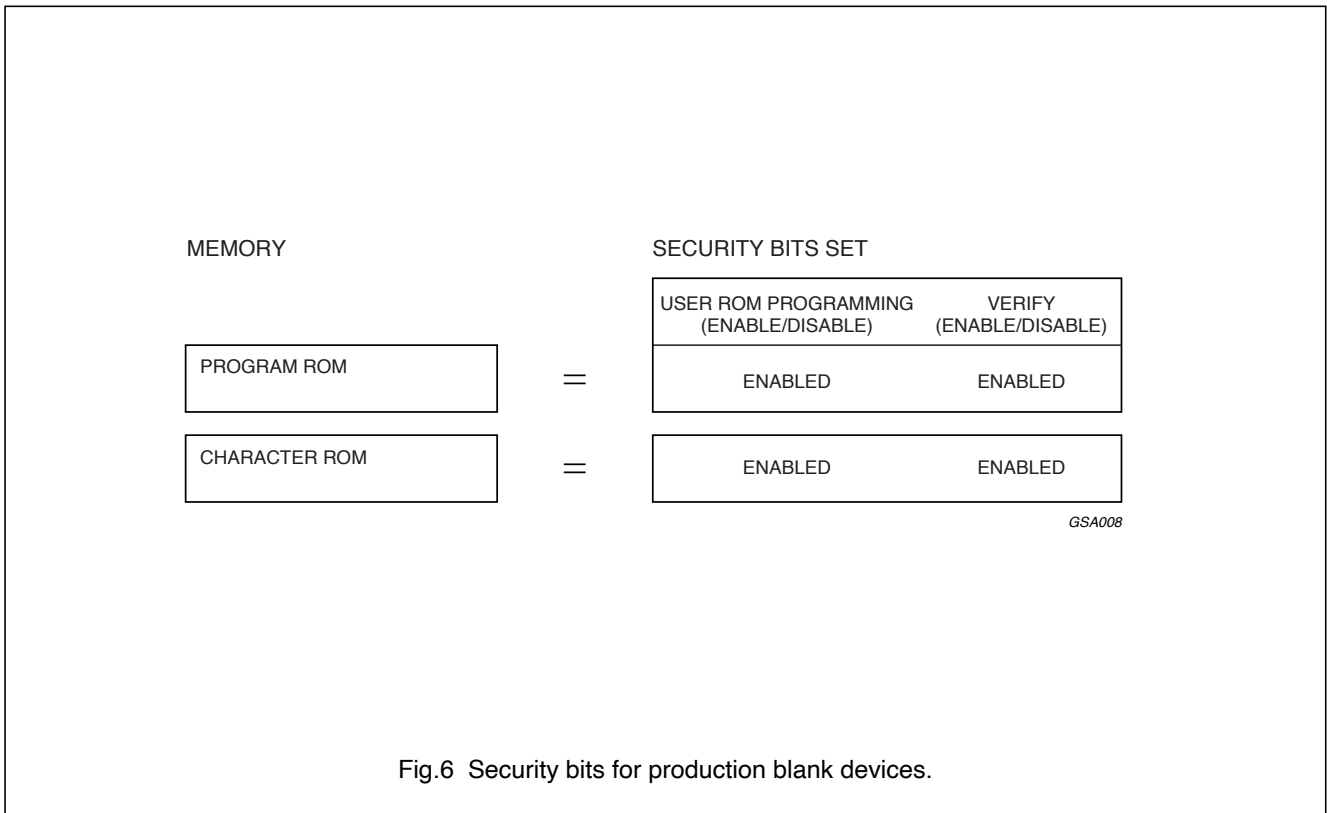
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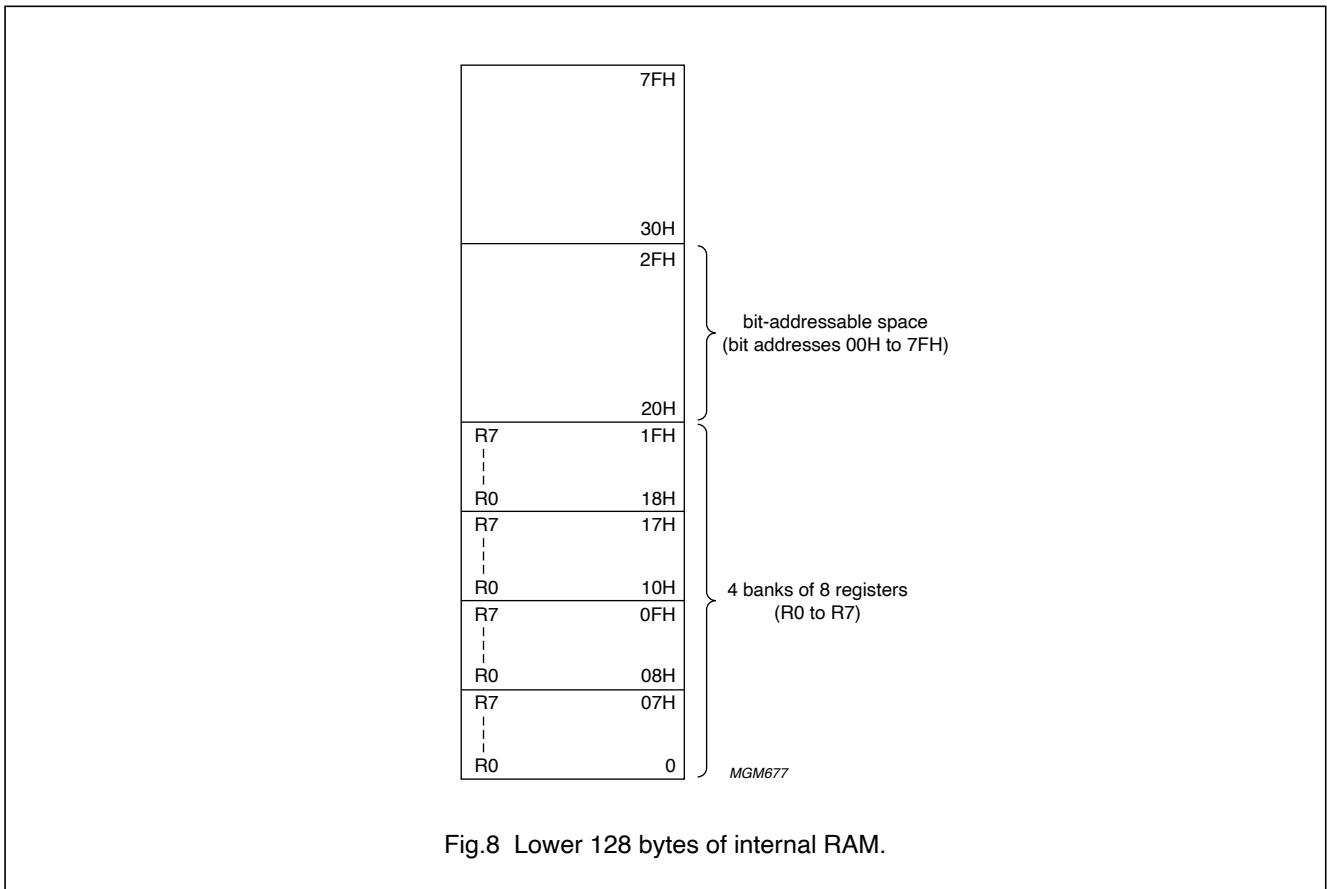
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8.4 SFR memory

The Special Function Register (SFR) space is used for port latches, timer, peripheral control, acquisition control, display control, etc. These registers can only be accessed by direct addressing. Sixteen of the addresses in the SFR space are both bit and byte addressable. The bit addressable SFRs are those whose address ends in 0H or 8H. A summary of the SFR map in address order is shown in Table 2.

A description of each of the SFR bits is shown in Table 3 which presents the SFRs in alphabetical order.

Table 2 SFR memory map

| ADD | R/W | NAME | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | RESET |
|-----|-----|--------|----------------|---------------|---------|---------|--------------------|----------|----------|----------|-------|
| 80H | R/W | PO | P07 | P06 | P05 | P04 | P03 | P02 | P01 | P00 | FFH |
| 81H | R/W | SP | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | 07H |
| 82H | R/W | DPL | DPL7 | DPL6 | DPL5 | DPL4 | DPL3 | DPL2 | DPL1 | DPL0 | 00H |
| 83H | R/W | DPH | DPH7 | DPH6 | DPH5 | DPH4 | DPH3 | DPH2 | DPH1 | DPH0 | 00H |
| 87H | R/W | PCON | 0 | ARD | RFI | WLE | GF1 | GF0 | PD | IDL | 00H |
| 88H | R/W | TCON | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | 00H |
| 89H | R/W | TMOD | GATE | C/T | M1 | M0 | GATE | C/T | M1 | M0 | 00H |
| 8AH | R/W | TL0 | TL07 | TL06 | TL05 | TL04 | TL03 | TL02 | TL01 | TL00 | 00H |
| 8BH | R/W | TL1 | TL17 | TL16 | TL15 | TL14 | TL13 | TL12 | TL11 | TL10 | 00H |
| 8CH | R/W | TH0 | TH07 | TH06 | TH05 | TH04 | TH03 | TH02 | TH01 | TH00 | 00H |
| 8DH | R/W | TH1 | TH17 | TH16 | TH15 | TH14 | TH13 | TH12 | TH11 | TH10 | 00H |
| 90H | R/W | P1 | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 | FFH |
| 96H | R/W | P0CFGA | P0CFGA7 | P0CFGA6 | P0CFGA5 | P0CFGA4 | P0CFGA3 | P0CFGA2 | P0CFGA1 | P0CFGA0 | FFH |
| 97H | R/W | P0CFGB | P0CFGB7 | P0CFGB6 | P0CFGB5 | P0CFGB4 | P0CFGB3 | P0CFGB2 | P0CFGB1 | P0CFGB0 | 00H |
| 98H | R/W | SADB | 0 | 0 | 0 | DC_COMP | SAD3 | SAD2 | SAD1 | SAD0 | 00H |
| 9EH | R/W | P1CFGA | P1CFGA7 | P1CFGA6 | P1CFGA5 | P1CFGA4 | P1CFGA3 | P1CFGA2 | P1CFGA1 | P1CFGA0 | FFH |
| 9FH | R/W | P1CFGB | P1CFGB7 | P1CFGB6 | P1CFGB5 | P1CFGB4 | P1CFGB3 | P1CFGB2 | P1CFGB1 | P1CFGB0 | 00H |
| A0H | R/W | P2 | P27 | P26 | P25 | P24 | P23 | P22 | P21 | P20 | FFH |
| A6H | R/W | P2CFGA | P2CFGA7 | P2CFGA6 | P2CFGA5 | P2CFGA4 | P2CFGA3 | P2CFGA2 | P2CFGA1 | P2CFGA0 | FFH |
| A7H | R/W | P2CFGB | P2CFGB7 | P2CFGB6 | P2CFGB5 | P2CFGB4 | P2CFGB3 | P2CFGB2 | P2CFGB1 | P2CFGB0 | 00H |
| A8H | R/W | IE | EA | EBUSY | ES2 | ECC | ET1 | EX1 | ET0 | EX0 | 00H |
| B0H | R/W | P3 | P37 | P36 | P35 | P34 | P33 | P32 | P31 | P30 | FFH |
| B2H | R/W | TXT18 | NOT3 | NOT2 | NOT1 | NOT0 | 0 | 0 | BS1 | BS0 | 00H |
| B3H | R/W | TXT19 | TEN | TC2 | TC1 | TC0 | 0 | 0 | TS1 | TS0 | 00H |
| B4H | R/W | TXT20 | DRCS ENABLE | OSD PLANES | 0 | 0 | OSD LANG ENABLE | OSD LAN2 | OSD LAN1 | OSD LAN0 | 00H |

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| ADD | R/W | NAME | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | RESET |
|-----|-----|--------|-----------------|-------------------|--------------|-----------------------|-------------------------|----------------|-------------------------|----------------------|-----------|
| B5H | R/W | TXT21 | DISP LINES1 | DISP LINES0 | CHAR SIZE1 | CHAR SIZE0 | I ² C PORT 1 | CC ON | I ² C PORT 0 | CC/TXT | 02H |
| B6H | R | TXT22 | GPF7 | GPF6 | GPF5 | GPF4 | GPF3 | GPF2 | GPF1 | GPF0 | XXH |
| B7H | R/W | CCLIN | 0 | 0 | 0 | CS4 | CS3 | CS2 | CS1 | CS0 | 15H |
| B8H | R/W | IP | 0 | PBUSY | PES2 | PCC | PT1 | PX1 | PT0 | PX0 | 00H |
| B9H | R/W | TXT17 | 0 | FORCE ACQ1 | FORCE ACQ0 | FORCE DISP1 | FORCE DISP0 | SCREEN COL2 | SCREEN COL1 | SCREEN COL0 | 00H |
| BEH | R/W | P3CFGA | P3CFGA7 | P3CFGA6 | P3CFGA5 | P3CFGA4 | P3CFGA3 | P3CFGA2 | P3CFGA1 | P3CFGA0 | FFH |
| BFH | R/W | P3CFGB | P3CFGB7 | P3CFGB6 | P3CFGB5 | P3CFGB4 | P3CFGB3 | P3CFGB2 | P3CFGB1 | P3CFGB0 | 00H |
| C0H | R/W | TXT0 | (reserved) 0 | (reserved) 0 | AUTO FRAME | (reserved) 0 | (reserved) 0 | DISABLE FRAME | (reserved) 0 | (reserved) 0 | 00H |
| C1H | R/W | TXT1 | (reserved) 0 | (reserved) 0 | (reserved) 0 | (reserved) 0 | (reserved) 0 | FIELD POLARITY | H POLARITY | V POLARITY | 00H |
| C4H | R/W | TXT4 | OSD BANK ENABLE | QUAD WIDTH ENABLE | EAST/WEST | DISABLE DOUBLE HEIGHT | B MESH ENABLE | C MESH ENABLE | TRANS ENABLE | SHADOW ENABLE | 00H |
| C5H | R/W | TXT5 | BKGND OUT | BKGND IN | COR OUT | COR IN | TEXT OUT | TEXT IN | PICTURE ON OUT | PICTURE ON IN | 03H |
| C6H | R/W | TXT6 | BKGND OUT | BKGND IN | COR OUT | COR IN | TEXT OUT | TEXT IN | PICTURE ON OUT | PICTURE ON IN | 03H |
| C7H | R/W | TXT7 | (reserved) 0 | CURSOR ON | (reserved) 0 | (reserved) 0 | DOUBLE HEIGHT | BOX ON 24 | BOX ON 1 – 23 | BOX ON 0 | 00H |
| C8H | R/W | TXT8 | (reserved) 0 | FLICKER STOP ON | (reserved) 0 | DISABLE SPANISH | PKT 26 RECEIVED | WSS RECEIVED | WSS ON | CVBS1/ CVBS0 | 00H |
| C9H | R/W | TXT9 | CURSOR FREEZE | CLEAR MEMORY | (reserved) 0 | R4 | R3 | R2 | R1 | R0 | 00H |
| CAH | R/W | TXT10 | 0 | 0 | C5 | C4 | C3 | C2 | C1 | C0 | 00H |
| CBH | R/W | TXT11 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00H |
| CCH | R | TXT12 | 525/625 SYNC | ROM VER4 | ROM VER3 | ROM VER2 | ROM VER1 | ROM VERO | 1 | VIDEO SIGNAL QUALITY | XXXX XX1X |
| D0H | R/W | PSW | C | AC | F0 | RS1 | RS0 | OV | - | P | 00H |
| D2H | R/W | TDACL | TD7 | TD6 | TD5 | TD4 | TD3 | TD2 | TD1 | TD0 | 00H |
| D3H | R/W | TDACH | TPWE | 1 | TD13 | TD12 | TD11 | TD10 | TD9 | TD8 | 40H |

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| ADD | R/W | NAME | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | RESET |
|-----|-----|--------|-----------------|------------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------|
| D4H | R/W | PWM7 | PW7E | 1 | PW7V5 | PW7V4 | PW7V3 | PW7V2 | PW7V1 | PW7V0 | 40H |
| D5H | R/W | PWM0 | PW0E | 1 | PW0V5 | PW0V4 | PW0V3 | PW0V2 | PW0V1 | PW0V0 | 40H |
| D6H | R/W | PWM1 | PW1E | 1 | PW1V5 | PW1V4 | PW1V3 | PW1V2 | PW1V1 | PW1V0 | 40H |
| D7H | R | CCDAT1 | CCD17 | CCD16 | CCD15 | CCD14 | CCD13 | CCD12 | CCD11 | CCD10 | 00H |
| D8H | R/W | S1CON | CR2 | ENSI | STA | STO | SI | AA | CR1 | CR0 | 00H |
| D9H | R | S1STA | STAT4 | STAT3 | STAT2 | STAT1 | STAT0 | 0 | 0 | 0 | F8H |
| DAH | R/W | S1DAT | DAT7 | DAT6 | DAT5 | DAT4 | DAT3 | DAT2 | DAT1 | DAT0 | 00H |
| DBH | R/W | S1ADR | ADR6 | ADR5 | ADR4 | ADR3 | ADR2 | ADR1 | ADR0 | GC | 00H |
| DCH | R/W | PWM3 | PW3E | 1 | PW3V5 | PW3V4 | PW3V3 | PW3V2 | PW3V1 | PW3V0 | 40H |
| DDH | R/W | PWM4 | PW4E | 1 | PW4V5 | PW4V4 | PW4V3 | PW4V2 | PW4V1 | PW4V0 | 40H |
| DEH | R/W | PWM5 | PW5E | 1 | PW5V5 | PW5V4 | PW5V3 | PW5V2 | PW5V1 | PW5V0 | 40H |
| DFH | R/W | PWM6 | PW6E | 1 | PW6V5 | PW6V4 | PW6V3 | PW6V2 | PW6V1 | PW6V0 | 40H |
| E0H | R/W | ACC | ACC7 | ACC6 | ACC5 | ACC4 | ACC3 | ACC2 | ACC1 | ACC0 | 00H |
| E4H | R/W | PWM2 | PW2E | 1 | PW2V5 | PW2V4 | PW2V3 | PW2V2 | PW2V1 | PW2V0 | 40H |
| E7H | R | CCDAT2 | CCD27 | CCD26 | CCD25 | CCD24 | CCD23 | CCD22 | CCD21 | CCD20 | 00H |
| E8H | R/W | SAD | VHI | CH1 | CH0 | ST | SAD7 | SAD6 | SAD5 | SAD4 | 00H |
| F0H | R/W | B | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 00H |
| F7H | W | WDTKEY | WKEY7 | WKEY6 | WKEY5 | WKEY4 | WKEY3 | WKEY2 | WKEY1 | WKEY0 | 00H |
| F8H | R/W | TXT13 | (reserved) 0 | PAGE CLEARING | 525 DISPLAY | (reserved) 0 | (reserved) 0 | (reserved) 0 | (reserved) 0 | (reserved) 0 | XXXX XXX0 |
| FAH | R/W | XRAMP | XRAMP7 | XRAMP6 | XRAMP5 | XRAMP4 | XRAMP3 | XRAMP2 | XRAMP1 | XRAMP0 | 00H |
| FBH | R/W | ROMBK | STANDBY | 0 | 0 | 0 | 0 | 0 | (reserved) 0 | (reserved) 0 | 00H |
| FFH | R/W | WDT | WDV7 | WDV6 | WDV5 | WDV4 | WDV3 | WDV2 | WDV1 | WDV0 | 00H |

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Table 3 SFR bit description

| BIT | FUNCTION |
|---|---|
| Accumulator (ACC) | |
| ACC7 to ACC0 | accumulator value |
| B Register (B) | |
| B7 to B0 | B register value |
| CC data byte 1 (CCDAT1) | |
| CCD17 to CCD10 | closed caption first data byte |
| CC data byte 2 (CCDAT2) | |
| CCD26 to CCD20 | closed caption second data byte |
| CC line (CCLIN) | |
| CS4 to CS0 | closed caption slice line using 525-line number |
| Data Pointer High byte (DPH) | |
| DPH7 to DPH0 | data pointer high byte, used with DPL to address auxiliary memory |
| Data pointer Low byte (DPL) | |
| DPL7 to DPL0 | data pointer low byte, used with DPH to address auxiliary memory |
| Interrupt Enable Register (IE) | |
| EA | disable all interrupts (logic 0), or use individual interrupt enable bits (logic 1) |
| EBUSY | enable BUSY interrupt |
| ES2 | enable I ² C-bus interrupt |
| ECC | enable closed caption interrupt |
| ET1 | enable Timer 1 interrupt |
| EX1 | enable external interrupt 1 |
| ET0 | enable Timer 0 interrupt |
| EX0 | enable external interrupt 0 |
| Interrupt Priority Register (IP) | |
| PBUSY | priority EBUSY interrupt |
| PES2 | priority ES2 Interrupt |
| PCC | priority ECC interrupt |
| PT1 | priority Timer 1 interrupt |
| PX1 | priority external interrupt 1 |
| PT0 | priority Timer 0 interrupt |
| PX0 | priority external interrupt 0 |
| Port 0 (P0) | |
| P07 to P00 | Port 0 I/O register connected to external pins |

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| BIT | FUNCTION |
|--|---|
| Port 1 (P1) | |
| P17 to P10 | Port 1 I/O register connected to external pins |
| Port 2 (P2) | |
| P27 to P20 | Port 2 I/O register connected to external pins |
| Port 3 (P3) | |
| P37 to P30 | Port 3 I/O register connected to external pins; P37 to P35 are only available with the LQFP100 package |
| Port 0 Configuration A (P0CFGA) and Port 0 Configuration B (P0CFGB) | |
| P0CFGA<7:0> and P0CFGB<7:0> | These two registers are used to configure Port 0 pins. For example, the I/O configuration of Port 0 pin 3 is controlled using bit 3 in both P0CFGA and P0CFGB. P0CFGB<x>/P0CFGA<x>: 00 = P0.x in open-drain configuration 01 = P0.x in quasi-bidirectional configuration 10 = P0.x in high-impedance configuration 11 = P0.x in push-pull configuration |
| Port 1 Configuration A (P1CFGA) and Port 1 Configuration B (P1CFGB) | |
| P1CFGA<7:0> and P1CFGB<7:0> | These two registers are used to configure Port 1 pins. For example, the I/O configuration of Port 1 pin 3 is controlled using bit 3 in both P1CFGA and P1CFGB. P1CFGB<x>/P1CFGA<x>: 00 = P1.x in open-drain configuration 01 = P1.x in quasi-bidirectional configuration 10 = P1.x in high-impedance configuration 11 = P1.x in push-pull configuration |
| Port 2 Configuration A (P2CFGA) and Port 2 Configuration B (P2CFGB) | |
| P2CFGA<7:0> and P2CFGB<7:0> | These two registers are used to configure Port 2 pins. For example, the I/O configuration of Port 2 pin 3 is controlled by using bit 3 in both P2CFGA and P2CFGB. P2CFGB<x>/P2CFGA<x>: 00 = P2.x in open-drain configuration 01 = P2.x in quasi-bidirectional configuration 10 = P2.x high-impedance configuration 11 = P2.x push-pull configuration |
| Port 3 Configuration A (P3CFGA) and Port 3 Configuration B (P3CFGB) | |
| P3CFGA<7:0> and P3CFGB<7:0> | These two registers are used to configure Port 3 pins. For example, the I/O configuration of Port 3 pin 3 is controlled using bit 3 in both P3CFGA and P3CFGB. P3CFGB<x>/P3CFGA<x>: 00 = P3.x in open-drain configuration 01 = P3.x in quasi-bidirectional configuration 10 = P3.x in high-impedance configuration 11 = P3.x in push-pull configuration |

TV microcontrollers with Closed Captioning (CC) and On-Screen Display (OSD)

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| BIT | FUNCTION |
|--|---|
| Power Control Register (PCON) | |
| ARD | auxiliary RAM disable, all MOVX instructions access the external data memory |
| RFI | disable ALE during internal access to reduce radio frequency interference |
| WLE | Watchdog Timer enable |
| GF1 | general purpose flag |
| GF0 | general purpose flag |
| PD | Power-down mode activation bit |
| IDL | Idle mode activation bit |
| Program Status Word (PSW) | |
| C | carry bit |
| AC | auxiliary carry bit |
| F0 | flag 0, general purpose flag |
| RS1 to RS0 | register bank selector bits; RS<1:0>: 00 = Bank 0 (00H to 07H) 01 = Bank 1 (08H to 0FH) 10 = Bank 2 (10H to 17H) 11 = Bank 3 (18H to 1FH) |
| OV | overflow flag |
| P | parity bit |
| Pulse Width Modulator 0 Control Register (PWM0) | |
| PW0E | activate this PWM (logic 1) |
| PW0V5 to PW0V0 | pulse width modulator high time |
| Pulse Width Modulator 1 Control Register (PWM1) | |
| PW1E | activate this PWM (logic 1) |
| PW1V5 to PW1V0 | pulse width modulator high time |
| Pulse Width Modulator 2 Control Register (PWM2) | |
| PW2E | activate this PWM (logic 1) |
| PW2V5 to PW2V0 | pulse width modulator high time |
| Pulse Width Modulator 3 Control Register (PWM3) | |
| PW3E | activate this PWM (logic 1) |
| PW3V5 to PW3V0 | pulse width modulator high time |
| Pulse Width Modulator 4 Control Register (PWM4) | |
| PW4E | activate this PWM (logic 1) |
| PW4V5 to PW4V0 | pulse width modulator high time |
| Pulse Width Modulator 5 Control Register (PWM5) | |
| PW5E | activate this PWM (logic 1) |
| PW5V5 to PW5V0 | pulse width modulator high time |

TV microcontrollers with Closed Captioning (CC) and On-Screen Display (OSD)

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| BIT | FUNCTION |
|--|--|
| Pulse Width Modulator 6 Control Register (PWM6) | |
| PW6E | activate this PWM (logic 1) |
| PW6V5 to PW6V0 | pulse width modulator high time |
| Pulse Width Modulator 7 Control Register (PWM7) | |
| PW7E | activate this PWM (logic 1) |
| PW7V5 to PW7V0 | pulse width modulator high time |
| ROM Bank (ROMBK) | |
| STBY | Standby mode enabled (logic 1) |
| I²C-bus Slave Address Register (S1ADR) | |
| ADR6 to ADR0 | I ² C-bus slave address to which the device will respond |
| GC | enable I ² C-bus general call address (logic 1) |
| I²C-bus Control Register (S1CON) | |
| CR2 to CR0 | clock rate bits; CR<2:0>: 000 = 100 kHz bit rate 001 = 3.75 kHz bit rate 010 = 150 kHz bit rate 011 = 200 kHz bit rate 100 = 25 kHz bit rate 101 = 1.875 kHz bit rate 110 = 37.5 kHz bit rate 111 = 50 kHz bit rate |
| ENSI | enable I ² C-bus interface (logic 1) |
| STA | START flag. When this bit is set in slave mode, the hardware checks the I ² C-bus and generates a START condition if the bus is free or after the bus becomes free. If the device operates in master mode it will generate a repeated START condition. |
| STO | STOP flag. If this bit is set in a master mode a STOP condition is generated. A STOP condition detected on the I ² C-bus clears this bit. This bit may also be set in slave mode in order to recover from an error condition. In this case no STOP condition is generated to the I ² C-bus, but the hardware releases the SDA and SCL lines and switches to the not selected receiver mode. The STOP flag is cleared by the hardware. |

TV microcontrollers with Closed Captioning (CC) and On-Screen Display (OSD)

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| BIT | FUNCTION |
|---|---|
| SI | <p>Serial Interrupt flag. This flag is set and an interrupt request is generated, after any of the following events occur:</p> <ul style="list-style-type: none"> • A START condition is generated in master mode • The own slave address has been received during AA = 1 • The general call address has been received while S1ADR.GC and AA = 1 • A data byte has been received or transmitted in master mode (even if arbitration is lost) • A data byte has been received or transmitted as selected slave • A STOP or START condition is received as selected slave receiver or transmitter. While the SI flag is set, SCL remains LOW and the serial transfer is suspended. SI must be reset by software. |
| AA | <p>Assert Acknowledge flag. When this bit is set, an acknowledge is returned after any one of the following conditions:</p> <ul style="list-style-type: none"> • Own slave address is received • General call address is received (S1ADR.GC = 1) • A data byte is received, while the device is programmed to be a master receiver • A data byte is received, while the device is selected slave receiver. <p>When the bit is reset, no acknowledge is returned. Consequently, no interrupt is requested when the own address or general call address is received.</p> |
| I²C-bus Data Register (S1DAT) | |
| DAT7 to DAT0 | I ² C-bus data |
| I²C-bus Status Register (S1STA) | |
| STAT4 to STAT0 | I ² C-bus interface status |
| Software ADC Register (SAD) | |
| VHI | analog input voltage greater than DAC voltage (logic 1) |
| CH1 to CH0 | ADC input channel select; CH<1:0>: 00 = ADC3 01 = ADC0 10 = ADC1 11 = ADC2 |
| ST ⁽¹⁾ | initiate voltage comparison between ADC input channel and SAD value |
| SAD7 to SAD4 | 4 MSBs of DAC input word |
| Software ADC Control Register (SADB) | |
| DC_COMP | enable DC comparator mode (logic 1) |
| SAD3 to SAD0 | 4 LSBs of SAD value |
| Stack Pointer (SP) | |
| SP7 to SP0 | stack pointer value |

TV microcontrollers with Closed Captioning (CC) and On-Screen Display (OSD)

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| BIT | FUNCTION |
|--|---|
| Timer/Counter Control Register (TCON) | |
| TF1 | Timer 1 overflow flag. Set by hardware on timer/counter overflow. Cleared by hardware when processor vectors to interrupt routine. |
| TR1 | Timer 1 run control bit. Set/cleared by software to turn timer/counter on/off. |
| TF0 | Timer 0 overflow flag. Set by hardware on timer/counter overflow. Cleared by hardware when processor vectors to interrupt routine. |
| TR0 | Timer 0 run control bit. Set/cleared by software to turn timer/counter on/off. |
| IE1 | Interrupt 1 edge flag (both edges generate flag). Set by hardware when external interrupt edge detected. Cleared by hardware when interrupt processed. |
| IT1 | Interrupt 1 type control bit. Set/cleared by software to specify edge/LOW level triggered external interrupts. |
| IE0 | Interrupt 0 edge I flag. Set by hardware when external interrupt edge detected. Cleared by hardware when interrupt processed. |
| IT0 | Interrupt 0 type flag. Set/cleared by software to specify falling edge/LOW level triggered external interrupts. |
| 14-bit PWM MSB Register (TDACH) | |
| TPWE | activate this 14-bit PWM (logic 1) |
| TD13 to TD8 | 6 MSBs of 14-bit number to be output by the 14-bit PWM |
| 14-bit PWM LSB Register (TDACL) | |
| TD7 to TD0 | 8 LSBs of 14-bit number to be output by the 14-bit PWM |
| Timer 0 High byte (TH0) | |
| TH07 to TH00 | Timer 0 high byte |
| Timer 1 High byte (TH1) | |
| TH17 to TH10 | Timer 1 high byte |
| Timer 0 Low byte (TL0) | |
| TL07 to TL00 | Timer 0 low byte |
| Timer 1 Low byte (TL1) | |
| TL17 to TL10 | Timer 1 low byte |
| Timer/Counter Mode Control (TMOD) | |
| GATE | gating control Timer/Counter 1 |
| C/\bar{T} | Counter/Timer 1 selector |
| M1 to M0 | mode control bits timer/counter 1; M<1:0>: 00 = 8-bit timer or 8-bit counter with divide-by-32 prescaler 01 = 16-bit time interval or event counter 10 = 8-bit time interval or event counter with automatic reload upon overflow; reload value stored in TH1 11 = stopped |
| GATE | gating control Timer/Counter 0 |
| C/\bar{T} | Counter/Timer 0 selector |

TV microcontrollers with Closed Captioning (CC) and On-Screen Display (OSD)

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| BIT | FUNCTION |
|-------------------------------|--|
| M1 to M0 | mode control bits timer/counter 0; M<1:0>: 00 = 8-bit timer or 8-bit counter with divide-by-32 prescaler 01 = 16-bit time interval or event counter 10 = 8-bit time interval or event counter with automatic reload upon overflow; reload value stored in TH0 11 = one 8-bit time interval or event counter and one 8-bit time interval counter |
| Text Register 0 (TXT0) | |
| AUTO FRAME | frame output is switched off automatically if any video displayed (logic 1) |
| DISABLE FRAME | force frame output to be LOW (logic 1) |
| Text Register 1 (TXT1) | |
| FIELD POLARITY | VSYNC pulse in second half of line during even field (logic 1) |
| H POLARITY | HSYNC reference edge is negative going (logic 1) |
| V POLARITY | VSYNC reference edge is negative going (logic 1) |
| Text Register 4 (TXT4) | |
| OSD BANK ENABLE | alternate OSD location available via graphic attribute, additional 32 location (logic 1) |
| QUAD WIDTH ENABLE | enable display of quadruple width characters (logic 1) |
| EAST/WEST | eastern character selection of character codes A0H to FFH (logic 1) |
| DISABLE DOUBLE HEIGHT | disable normal decoding of double height characters (logic 1) |
| B MESH ENABLE | enable meshing of black background (logic 1) |
| C MESH ENABLE | enable meshing of coloured background (logic 1) |
| TRANS ENABLE | display black background as video (logic 1) |
| SHADOW ENABLE | display shadow/fringe (default SE black) (logic 1) |
| Text Register 5 (TXT5) | |
| BKGND OUT | background colour displayed outside teletext boxes (logic 1) |
| BKGND IN | background colour displayed inside teletext boxes (logic 1) |
| COR OUT | COR active outside teletext and OSD boxes (logic 1) |
| COR IN | COR active inside teletext and OSD boxes (logic 1) |
| TEXT OUT | text displayed outside teletext boxes (logic 1) |
| TEXT IN | text displayed inside teletext boxes (logic 1) |
| PICTURE ON OUT | video displayed outside teletext boxes (logic 1) |
| PICTURE ON IN | video displayed inside teletext boxes (logic 1) |
| Text Register 6 (TXT6) | |
| BKGND OUT | background colour displayed outside teletext boxes (logic 1) |
| BKGND IN | background colour displayed inside teletext boxes (logic 1) |
| COR OUT | COR active outside teletext and OSD boxes (logic 1) |
| COR IN | COR active inside teletext and OSD boxes (logic 1) |
| TEXT OUT | text displayed outside teletext boxes (logic 1) |
| TEXT IN | text displayed inside teletext boxes (logic 1) |
| PICTURE ON OUT | video displayed outside teletext boxes (logic 1) |

TV microcontrollers with Closed Captioning (CC) and On-Screen Display (OSD)

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| BIT | FUNCTION |
|---------------------------------|---|
| PICTURE ON IN | video displayed inside teletext boxes (logic 1) |
| Text Register 7 (TXT7) | |
| CURSOR ON | display cursor at position given by TXT9 and TXT10 (logic 1) |
| DOUBLE HEIGHT | display each character as twice normal height (logic 1) |
| BOX ON 24 | enable display of teletext boxes in memory row 24 (logic 1) |
| BOX ON 1 – 23 | enable display of teletext boxes in memory row 1 to 23 (logic 1) |
| BOX ON 0 | enable display of teletext boxes in memory row 0 (logic 1) |
| Text Register 8 (TXT8) | |
| FLICKER STOP ON | disable 'Flicker Stopper' circuitry (logic 1) |
| DISABLE SPANISH | disable special treatment of Spanish packet 26 characters (logic 1) |
| PKT 26 RECEIVED ⁽²⁾ | packet 26 data has been processed (logic 1) |
| WSS RECEIVED ⁽²⁾ | wide screen signalling data has been processed (logic 1) |
| WSS ON | enable acquisition of WSS data (logic 1) |
| CVBS1/CVBS0 | select CVBS1 as source for device (logic 1) |
| Text Register 9 (TXT9) | |
| CURSOR FREEZE | lock cursor at current position (logic 1) |
| CLEAR MEMORY ⁽¹⁾ | clear memory block pointed to by TXT15 |
| R4 to R0 ⁽²⁾ | current memory row value |
| Text Register 10 (TXT10) | |
| C5 to C0 ⁽³⁾ | current memory column value |
| Text Register 11 (TXT11) | |
| D7 to D0 | data value written or read from memory location defined by TXT9, TXT10 and TXT15 |
| Text Register 12 (TXT12) | |
| 525/625 SYNC ⁽⁴⁾ | 525-line CVBS signal is being received (logic 1) |
| ROM VER4 to ROM VER0 | mask programmable identification for character set |
| VIDEO SIGNAL QUALITY | acquisition can be synchronised to CVBS (logic 1) |
| Text Register 13 (TXT13) | |
| PAGE CLEARING | software or power-on page clear in progress (logic 1) |
| 525 DISPLAY | 525-line synchronisation for display (logic 1) |
| Text Register 17 (TXT17) | |
| FORCE ACQ1 to FORCE ACQ0 | FORCE ACQ<1:0>: 00 = automatic selection 01 = force 525 timing, force 525 teletext standard 10 = force 625 timing, force 625 teletext standard 11 = force 625 timing, force 525 teletext standard |

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| BIT | FUNCTION |
|---------------------------------|---|
| FORCE DISP1 to FORCE DISP0 | FORCE DISP<1:0>: 00 = automatic selection 01 = force display to 525 mode (9 lines per row) 10 = force display to 625 mode (10 lines per row) 11 = not valid (default to 625 mode) |
| SCREEN COL2 to SCREEN COL0 | Defines colour to be displayed instead of TV picture and black background; these bits are equivalent to the RGB components. SCREEN COL<2:0>: 000 = transparent 001 = CLUT entry 9 010 = CLUT entry 10 011 = CLUT entry 11 100 = CLUT entry 12 101 = CLUT entry 13 110 = CLUT entry 14 111 = CLUT entry 15 |
| Text Register 18 (TXT18) | |
| NOT3 to NOT0 | national option table selection, maximum of 31 when used with EAST/WEST bit |
| BS1 to BS0 | basic character set selection |
| Text Register 19 (TXT19) | |
| TEN | enable twist character set (logic 1) |
| TC2 to TC0 | language control bits (C12, C13 and C14) that has twisted character set |
| TS1 to TS0 | twist character set selection |
| Text Register 20 (TXT20) | |
| DRCS ENABLE | re-map column 9 to DRCS in TXT mode (logic 1) |
| OSD PLANES | character code columns 8 and 9 defined as double plane characters (logic 1) |
| OSD LANG ENABLE | enable use of OSD LAN<2:0> to define language option for display, instead of C12, C13 and C14 |
| OSD LAN2 to OSD LAN0 | alternative C12, C13 and C14 bits for use with OSD menus |
| Text Register 21 (TXT21) | |
| DISP LINES1 to DISP LINES0 | the number of display lines per character row; DISP LINES<1:0>: 00 = 10 lines per character (defaults to 9 lines in 525 mode) 01 = 13 lines per character 10 = 16 lines per character 11 = reserved (logic 1) |
| CHAR SIZE1 to CHAR SIZE0 | character matrix size; CHAR SIZE<1:0>: 00 = 10 lines per character (matrix 12 × 10) 01 = 13 lines per character (matrix 12 × 13) 10 = 16 lines per character (matrix 12 × 16) 11 = reserved |
| I ² C PORT 1 | enable I ² C-bus Port 1 selection (P1.5/SDA1 and P1.4/SCL1) (logic 1) |

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| BIT | FUNCTION |
|------------------------------------|--|
| CC ON | closed caption acquisition on (logic 1) |
| I ² C PORT 0 | enable I ² C-bus Port 0 selection (P1.7/SDA0 and P1.6/SCL0) (logic 1) |
| CC/TXT | display configured for CC mode (logic 1) |
| Text Register 22 (TXT22) | |
| GPF7 to GPF5 | general purpose register, bits defined by mask programmable bits |
| GPF4 | reserved |
| GPF3 | PWM0, PWM1, PWM2 and PWM3 output on Port 2.1 to Port 2.4 respectively (logic 1) |
| GPF2 | enable closed caption acquisition (logic 1) |
| GPF1 and GPF0 | reserved |
| Watchdog Timer (WDT) | |
| WDV7 to WDV0 | Watchdog Timer period |
| Watchdog Timer Key (WDTKEY) | |
| WKEY7 to WKEY0 ⁽⁵⁾ | Watchdog Timer Key value |
| XRAMP | |
| XRAMP7 to XRAMP0 | internal RAM access upper byte address |

Notes

1. This flag is set by software and reset by hardware.
2. Valid range TXT mode 0 to 24.
3. Valid range TXT mode 0 to 39.
4. Only valid when VIDEO SIGNAL QUALITY is set.
5. Must be set to 55H to disable Watchdog Timer when active.

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8.5 Character set feature bits

Features available on the OSD only devices are reflected in a specific area of the Character ROM. These sections of the Character ROM are mapped to two Special Function Registers: TXT22 and TXT12. Character ROM address 09FEH is mapped to SFR TXT22 as shown in Table 4. Character ROM address 09FFH is mapped to SFR TXT12 as shown in Table 6.

Table 4 Character ROM - TXT22 mapping

U = used; X = reserved

| MAPPED ITEMS | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------------------|----|----|---|---|---|---|---|---|---|---|---|---|
| Character ROM address 09FEH | X | X | X | X | X | X | X | X | U | U | X | X |
| Mapped to TXT22 | - | - | - | - | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Table 5 Description of Character ROM address 09FEH bits

| BIT | DESCRIPTION |
|---------|--|
| 0 to 1 | reserved; normally all set to logic 1 |
| 2 | 1 = enable CC acquisition 0 = disable CC acquisition |
| 3 | 1 = PWM0, PWM1, PWM2 and PWM3 output routed to Port 2.1 to Port 2.4 respectively 0 = PWM0, PWM1, PWM2 and PWM3 output routed to Port 3.0 to Port 3.3 respectively |
| 4 to 11 | reserved; normally all set to logic 1 |

Table 6 Character ROM - TXT12 mapping

U = used; X = reserved

| MAPPED ITEMS | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------------------|----|----|---|---|---|---|---|---|---|---|---|---|
| Character ROM address 09FFH | X | X | X | X | X | X | X | X | X | X | X | X |
| Mapped to TXT12 | - | - | - | - | - | - | - | 6 | 5 | 4 | 3 | 2 |

Table 7 Description of Character ROM address 09FFH bits

| BIT | DESCRIPTION |
|---------|---------------------------------------|
| 0 to 11 | reserved; normally all set to logic 1 |

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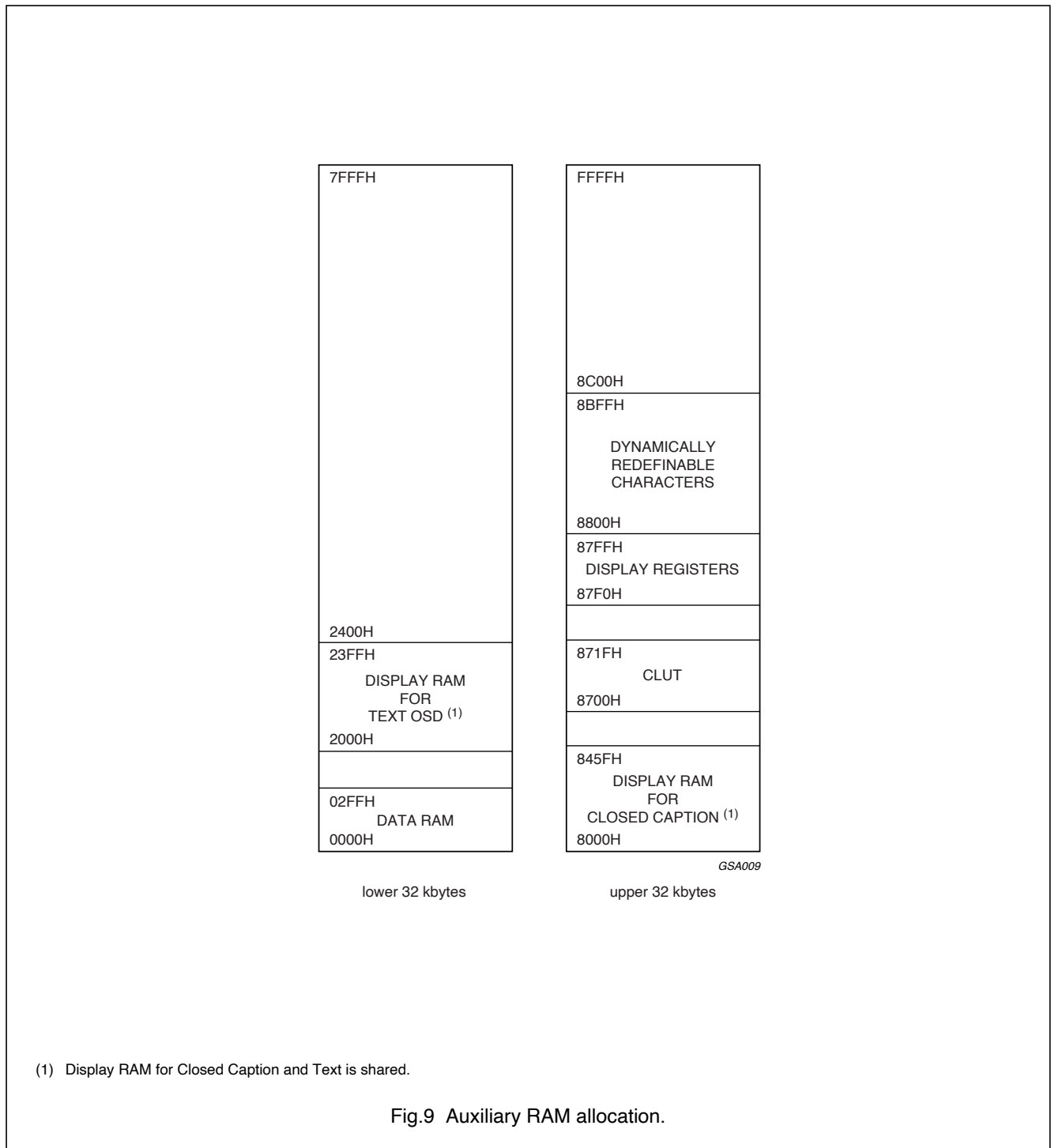
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8.6 External (auxiliary) memory

The normal 80C51 external memory area has been mapped internally to the device, this means that the MOVX instruction accesses memory internal to the device.

8.6.1 AUXILIARY RAM PAGE SELECTION

The Auxiliary RAM page pointer is used to select one of the 256 pages within the Auxiliary RAM, not all pages are allocated; refer to Fig.9 for further detail. A page consists of 256 consecutive bytes.



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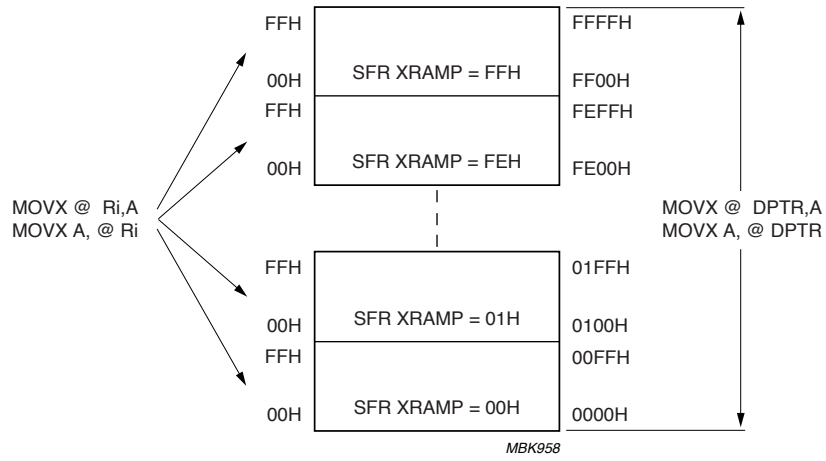


Fig.10 Indirect addressing of Auxiliary RAM.

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9 REDUCED POWER MODES

There are three power saving modes: Standby, Idle and Power-down, incorporated into the OSD only device. When utilizing any of these modes, power to the device (V_{DDP} , V_{DDC} and V_{DDA}) should be maintained, since power saving is achieved by clock gating on a section by section basis.

9.1 Idle mode

During Idle mode, Acquisition, Display and the Central Processing Unit (CPU) sections of the device are disabled. The following functions remain active:

- Memory interface
- I²C-bus interface
- Timer/Counters
- Watchdog Timer
- Pulse Width Modulators.

To enter Idle mode the IDL bit in the PCON register must be set. The Watchdog Timer must be disabled prior to entering the Idle mode to prevent the device being reset. Once in Idle mode, the crystal oscillator continues to run, but the internal clock to the CPU, Acquisition and Display are gated out. However, the clocks to the Memory interface, I²C-bus interface, timer/counters, Watchdog Timer and Pulse Width Modulators are maintained. The CPU state is frozen along with the status of all SFRs, internal RAM contents are maintained, as are the device output pin values.

Since the output values on Red Green Blue (RGB) and the Video Data Switch (VDS) are maintained the display output must be disabled before entering this mode.

There are three methods to recover from Idle mode:

- Assertion of an enabled interrupt will cause the IDL bit to be cleared by hardware, thus terminating Idle mode. The interrupt is serviced, and following the instruction RETI, the next instruction to be executed will be the one after the instruction that put the device into Idle mode.
- A second method of exiting the Idle mode is via an interrupt generated by the Software Analog-to-Digital (SAD) DC Compare circuit. When the device is configured in this mode, detection of an analog threshold at the input to the SAD may be used to trigger wake-up of the device i.e. TV Front Panel Key-press. As above, the interrupt is serviced, and following the instruction RETI, the next instruction to be executed will be the one following the instruction that put the device into Idle mode.

- The third method of terminating Idle mode is with an external hardware reset. Since the oscillator is running, the hardware reset need only be active for two machine cycles (24 clocks at 12 MHz) to complete the reset operation. Reset defines all SFRs and Display memory to an initialized state, but maintains all other RAM values. Code execution commences with the Program Counter set to '0000'.

9.2 Power-down mode

In Power-down mode the crystal oscillator is stopped. The contents of all SFRs and Data memory are maintained. However, the contents of the Auxiliary/Display memory are lost. The port pins maintain the values defined by their associated SFRs. Since the output values on RGB and VDS are maintained the display output must be made inactive before entering Power-down mode.

The Power-down mode is activated by setting the PD bit in the PCON register. It is advised to disable the Watchdog Timer prior to entering Power-down.

There are three methods of exiting Power-down mode:

- An external interrupt provides the first mechanism for waking from Power-down. Since the clock is stopped, external interrupts need to be set level sensitive prior to entering Power-down. The interrupt is serviced, and following the instruction RETI, the next instruction to be executed will be the one after the instruction that put the device into Power-down mode.
- A second method of exiting power-down is via an interrupt generated by the SAD DC Compare circuit. When the device is configured in this mode, detection of a certain analog threshold at the input to the SAD may be used to trigger wake-up of the device i.e. TV Front Panel Key-press. As above, the interrupt is serviced, and following the instruction RETI, the next instruction to be executed will be the one following the instruction that put the device into the Power-down.
- The third method of terminating the Power-down mode is with an external hardware reset. Reset defines all SFRs and Display memory, but maintains all other RAM values. Code execution commences with the Program Counter set to '0000'.

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9.3 Standby mode

When Standby mode is entered both Acquisition and Display sections are disabled. The following functions remain active:

- 80C51 core
- Memory interface
- I²C-bus interface
- Timer/Counters
- Watchdog Timer
- Software ADC
- Pulse Width Modulators

To enter Standby mode, the STANDBY control bit in the ROMBK SFR (bit 7) must be set. It can be used in conjunction with either Idle or Power-down modes to switch between power saving modes. This mode enables the 80C51 core to decode either IR remote commands or receive I²C-bus commands without the device being fully powered.

The Standby state is maintained upon exit from either the Idle mode or Power-down mode. No wake-up from Standby is necessary as the 80C51 core remains operational.

Since the output values on RGB and VDS are maintained the display output must be disabled before entering this mode.

10 I/O FACILITY

10.1 I/O ports

The SAA55xx devices have 29 I/O lines, each is individually addressable, or form 3 parallel 8-bit addressable ports which are Port 0, Port 1 and Port 2. Port 3 has 5-bit parallel I/Os only.

10.2 Port type

All individual ports can be programmed to function in one of four I/O configurations: open-drain, quasi-bidirectional, high-impedance and push-pull. The I/O configuration is selected using two associated Port Configuration Registers: PnCFGA and PnCFGB (where n = port number 0, 1, 2 or 3); see Table 3.

10.2.1 OPEN-DRAIN

The open-drain configuration can be used for bidirectional operation of a port. It requires an external pull-up resistor, the pull-up voltage has a maximum value of 5.5 V, to allow connection of the device into a 5 V environment.

Note that the I²C-bus ports (P1.4, P1.5, P1.6 and P1.7) can only be configured as open-drain.

10.2.2 QUASI-BIDIRECTIONAL

The quasi-bidirectional configuration is a combination of open-drain and push-pull. It requires an external pull-up resistor to V_{DDP} (nominally 3.3 V). When a signal transition from LOW-to-HIGH is output from the device, the pad is put into push-pull configuration for one clock cycle (166 ns) after which the pad goes into open-drain configuration. This configuration is used to speed up the edges of signal transitions. This is the default state of operation of the pads after reset.

10.2.3 HIGH-IMPEDANCE

The high-impedance configuration can be used for input only operation of the port. When using this configuration the two output transistors are turned off.

10.2.4 PUSH-PULL

The push-pull configuration can be used for output only. In this configuration the signal is driven to either 0 V or V_{DDP}, which is nominally 3.3 V.

10.3 Port alternative functions

Ports 1, 2 and 3 are shared with alternative functions to enable control of external devices and circuitry. The alternative functions are enabled by setting the appropriate SFR and also writing a logic 1 to the port bit that the function occupies.

10.4 LED support

Port pins P0.5 and P0.6 have a 8 mA current sinking capability to enable LEDs in series with current limiting resistors to be driven directly, without the need for additional buffering circuitry.

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11 INTERRUPT SYSTEM

The device has six interrupt sources, each of which can be enabled or disabled. When enabled each interrupt can be assigned one of two priority levels. There are four interrupts that are common to the 80C51, two of these are external interrupts (EX0 and EX1) and the other two are timer interrupts (ET0 and ET1). In addition to the conventional 80C51, one application specific interrupt is incorporated internal to the device which has following functionality:

- **Display Busy interrupt (EBUSY).** An interrupt is generated when the display enters either a Horizontal or Vertical Blanking Period. i.e. indicates when the microcontroller can update the display RAM without causing undesired effects on the screen. This interrupt can be configured in one of two modes using the MMR Configuration (address 87FFH, bit TXT/V):
 - Text Display Busy. An interrupt is generated on each active horizontal display line when the Horizontal Blanking Period is entered
 - Vertical Display Busy. An interrupt is generated on each vertical display field when the Vertical Blanking period is entered.

11.1 Interrupt enable structure

Each of the individual interrupts can be enabled or disabled by setting or clearing the relevant bit in the Interrupt Enable Register (IE). All interrupt sources can also be globally disabled by clearing the EA bit (IE.7).

11.2 Interrupt enable priority

Each interrupt source can be assigned one of two priority levels. The interrupt priorities are defined by the Interrupt Priority Register (IP). A low priority interrupt can be interrupted by a high priority interrupt, but not by another low priority interrupt. A high priority interrupt can not be interrupted by any other interrupt source. If two requests of different priority level are received simultaneously, the request with the highest priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus, within each priority level there is a second priority structure determined by the polling sequence as defined in Table 8.

Table 8 Interrupt priority (within same level)

| SOURCE | PRIORITY WITHIN LEVEL | INTERRUPT VECTOR |
|--------|-----------------------|------------------|
| EX0 | highest | 0003H |
| ET0 | – | 000BH |
| EX1 | – | 0013H |
| ET1 | – | 001BH |
| ES2 | – | 002BH |
| EBUSY | lowest | 0033H |

11.3 Interrupt vector address

The processor acknowledges an interrupt request by executing a hardware generated LCALL to the appropriate servicing routine. The interrupt vector addresses for each source are shown in Table 8.

11.4 Level/edge interrupt

The external interrupt can be programmed to be either level-activated or transition-activated by setting or clearing the IT0/IT1 bits in the Timer Control SFR (TCON).

Table 9 External interrupt activation

| ITx | LEVEL | EDGE |
|-----|------------|---|
| 0 | active LOW | – |
| 1 | – | INT0 = negative edge INT1 = positive and negative edge |

The external interrupt INT1 differs from the standard 80C51 interrupt in that it is activated on both edges when in edge sensitive mode. This is to allow software pulse width measurement for handling remote control inputs.

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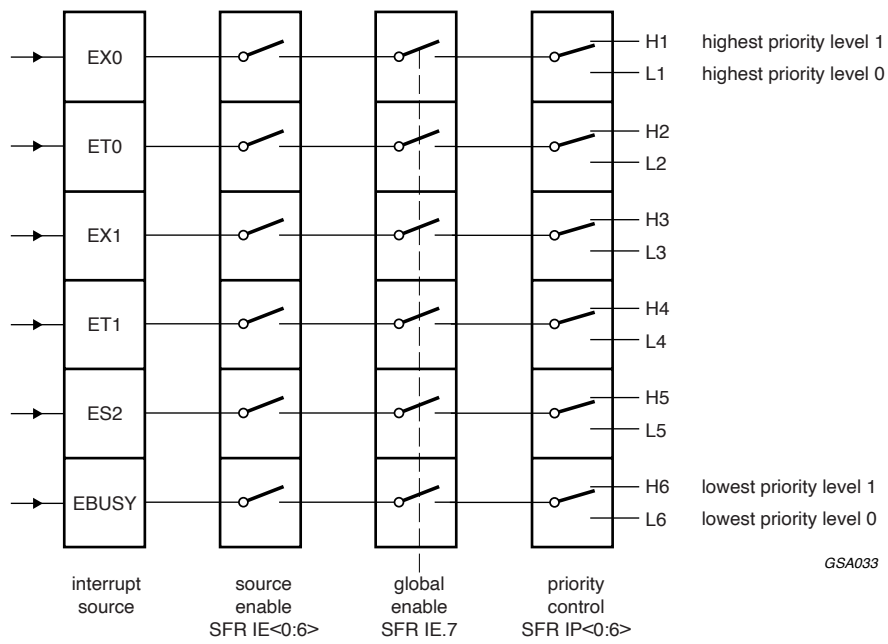


Fig.11 Interrupt structure.

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12 TIMER/COUNTER

Two 16-bit timers/counters are incorporated Timer 0 and Timer 1. Both can be configured to operate as either timers or event counters.

In Timer mode, the register is incremented on every machine cycle. It is therefore counting machine cycles. Since the machine cycle consists of twelve oscillator periods, the count rate is $\frac{1}{12}f_{osc} = 1$ MHz.

In Counter mode, the register is incremented in response to a negative transition at its corresponding external pin T0 or T1. Since the pins T0 and T1 are sampled once per machine cycle, it takes two machine cycles to recognise a transition, this gives a maximum count rate of $\frac{1}{24}f_{osc} = 0.5$ MHz.

There are six Special Function Registers used to control the timers/counters. These are: TCON, TMOD, TL0, TH0, TL1 and TH1.

The timer/counter function is selected by control bits C/T in the Timer Mode SFR (TMOD). These two Timer/Counters have four operating modes, which are selected by bit-pairs (M1 and M0) in TMOD. Detail of the modes of operation is given in *"Handbook IC20, 80C51-Based 8-bit Microcontrollers"*.

TL0 and TH0 are the actual Timer/Counter registers for Timer 0. TL0 is the low byte and TH0 is the high byte. TL1 and TH1 are the actual Timer/Counter registers for Timer 1. TL1 is the low byte and TH1 is the high byte.

13 WATCHDOG TIMER

The Watchdog Timer is a counter that once in an overflow state forces the microcontroller into a reset condition. The purpose of the Watchdog Timer is to reset the microcontroller if it enters an erroneous processor state (possibly caused by electrical noise or RFI) within a reasonable period of time. When enabled, the Watchdog circuitry will generate a system reset if the user program fails to reload the Watchdog Timer within a specified length of time known as the Watchdog Interval (WI).

The Watchdog Timer consists of an 8-bit counter with an 11-bit prescaler. The prescaler is fed with a signal whose frequency is $\frac{1}{12}f_{osc}$ (1 MHz for 12 MHz oscillator).

The 8-bit timer is incremented every 't' seconds where:

$$t = 12 \times 2048 \times \frac{1}{f_{osc}} = 12 \times 2048 \times \frac{1}{12 \times 10^6} = 2.048 \text{ ms}$$

13.1 Watchdog Timer operation

The Watchdog operation is activated when the WLE bit in the Power Control SFR (PCON) is set. The Watchdog can be disabled by software by loading the value 55H into the Watchdog Timer Key SFR (WDTKEY). This must be performed before entering the Idle or Power-down mode to prevent exiting the mode prematurely.

Once activated the Watchdog Timer SFR (WDT) must be reloaded before the timer overflows. The WLE bit must be set to enable loading of the WDT SFR, once loaded the WLE bit is reset by hardware, this is to prevent erroneous software from loading the WDT SFR.

The value loaded into the WDT defines the Watchdog Interval (WI).

$$WI = (256 - WDT) \times t = (256 - WDT) \times 2.048 \text{ ms}$$

The range of intervals is from WDT = 00H which gives 524 ms to WDT = FFH which gives 2.048 ms.

14 PULSE WIDTH MODULATORS

The device has eight 6-bit Pulse Width Modulated (PWM) outputs for analog control of e.g. volume, balance, bass, treble, brightness, contrast, hue and saturation. The PWM outputs generate pulse patterns with a repetition rate of 21.33 μ s, with the high time equal to the PWM SFR value multiplied by 0.33 μ s. The analog value is determined by the ratio of the high time to the repetition time, a D.C. voltage proportional to the PWM setting is obtained by means of an external integration network (low-pass filter).

14.1 PWM control

The relevant PWM is enabled by setting the PWM enable bit PWxE in the PWMx Control Register (where x = 0 to 7). The high time is defined by the value PWxV<5:0>.

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14.2 Tuning Pulse Width Modulator (TPWM)

The device has a single 14-bit PWM that can be used for Voltage Synthesis Tuning. The method of operation is similar to the normal PWM except that the repetition period is 42.66 μ s.

14.3 TPWM control

Two SFRs are used to control the TPWM, they are TDACL and TDACH. The TPWM is enabled by setting the TPWE bit in the TDACH SFR. The most significant bits TD<13:7> alter the high period between 0 and 42.33 μ s. The seven least significant bits TD<6:0> extend certain pulses by a further 0.33 μ s, e.g. if TD<6:0> = 01H then 1 in 128 periods will be extended by 0.33 μ s, if TD<6:0> = 02H then 2 in 128 periods will be extended.

The TPWM will not start to output a new value until TDACH has been written to. Therefore, if the value is to be changed, TDACL should be written before TDACH.

14.4 Software ADC (SAD)

Four successive approximation Analog-to-Digital Converters can be implemented in software by making use of the on-board 8-bit Digital-to-Analog Converter and Analog Comparator.

14.4.1 SAD CONTROL

The control of the required analog input is done using the channel select bits CH<1:0> in the SAD SFR, this selects the required analog input to be passed to one of the inputs of the comparator. The second comparator input is generated by the DAC whose value is set by the bits SAD<7:0> in the SAD and SADB SFRs. A comparison between the two inputs is made when the start compare bit ST in the SAD SFR is set, this must be at least one instruction cycle after the SAD<7:0> value has been set. The result of the comparison is given on VHI one instruction cycle after the setting of ST.

14.4.2 SAD INPUT VOLTAGE

The external analog voltage that is used for comparison with the internally generated DAC voltage does not have the same voltage range. The DAC has a lower reference level of V_{SSA} and an upper reference level of V_{DDP} .

The resolution of the DAC voltage with a nominal value is $3.3/256 \approx 13$ mV. The external analog voltage has a lower value equivalent to V_{SSA} and an upper value equivalent to $V_{DDP} - V_{tn}$, where V_{tn} is the threshold voltage for an N type Metal Oxide Semiconductor transistor. The reason for this is that the input pins for the analog signals (P3.0 to P3.3) are 5 V tolerant for normal port operations, i.e. when not used as analog input. To protect the analog multiplexer and comparator circuitry from the 5 V, a series transistor is used to limit the voltage. This limiting introduces a voltage drop equivalent to V_{tn} (≈ 0.6 V) on the input voltage. Therefore, for an input voltage in the range V_{DDP} to $V_{DDP} - V_{tn}$ the SAD returns the same comparison value.

14.4.3 SAD DC COMPARATOR MODE

The SAD module incorporates a DC Comparator mode which is selected using the DC_COMP control bit in the SADB SFR. This mode enables the microcontroller to detect a threshold crossing at the input to the selected analog input pin (P3.0/ADC0, P3.1/ADC1, P3.2/ADC2 or P3.3/ADC3) of the software ADC. A level sensitive interrupt is generated when the analog input voltage level at the pin falls below the analog output level of the SAD DAC.

This mode is intended to provide the device with a wake-up mechanism from Power-down or Idle mode when a key-press on the front panel of the TV is detected.

The following software sequence should be used when utilizing this mode for Power-down or Idle:

1. Disable INT1 using the IE SFR.
2. Set INT1 to level sensitive using the TCON SFR.
3. Set the DAC digital input level to the desired threshold level using SAD/SADB SFRs and select the required input pin (P3.0/ADC0, P3.1/ADC1, P3.2/ADC2 or P3.3/ADC3) using CH<1:0> in the SAD SFR.
4. Enter DC Compare mode by setting the DC_COMP enable bit in the SADB SFR.
5. Enable INT1 using the IE SFR.
6. Enter Power-down/Idle mode. Upon wake-up the SAD should be restored to its conventional operating mode by disabling the DC_COMP control bit.

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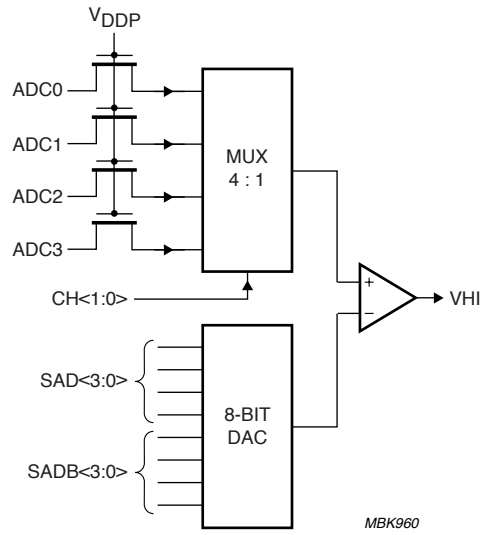


Fig.12 SAD block diagram.

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15 I²C-BUS SERIAL I/O

The I²C-bus consists of a serial data (SDA) line and a serial clock (SCL) line. The definition of the I²C-bus protocol can be found in the document "*The I²C-bus and how to use it (including specification)*". This document may be ordered using the code 9398 393 40011.

The device operates in four modes:

- Master transmitter
- Master receiver
- Slave transmitter
- Slave receiver.

The microcontroller peripheral is controlled by the Serial Control SFR (S1CON) and its status is indicated by the Status SFR (S1STA). Information is transmitted/received to/from the I²C-bus using the Data SFR (S1DAT) and the Slave Address SFR (S1ADR) is used to configure the slave address of the peripheral.

The byte level I²C-bus serial port is identical to the I²C-bus serial port on the P8xCE558, except for the clock rate selection bits CR<2:0> in S1CON. The operation of the subsystem is described in detail in the "*P8xCE558 data sheet*".

15.1 I²C-bus port selection

Two I²C-bus ports are available SCL0/SDA0 and SCL1/SDA1. The selection of the port is done using TXT21.I²C PORT 0 and TXT21.I²C PORT 1. When the port is enabled, any information transmitted from the device goes onto the enabled port. Any information transmitted to the device can only be acted on if the port is enabled.

If both ports are enabled then data transmitted from the device is seen on both ports, however data transmitted to the device on one port can not be seen on the other port.

16 MEMORY INTERFACE

The memory interface controls access to the embedded DRAM, refreshing of the DRAM and page clearing. The DRAM is shared between Data Capture, display and microcontroller sections.

The Data Capture section uses the DRAM to store acquired information that has been requested. The display reads from the DRAM information and converts it into RGB values. The microcontroller uses the DRAM as embedded auxiliary RAM.

16.1 Memory structure

The memory is partitioned into two distinct areas, the dedicated Auxiliary RAM area, and the Display RAM area. The Display RAM area when not being used for Data Capture or Display can be used as an extension to the auxiliary RAM area.

16.1.1 AUXILIARY RAM

The Auxiliary RAM is not initialised at power-up. The contents of the Auxiliary RAM area, and the Display RAM are maintained during Standby and Idle modes, but are lost if Power-down mode is entered.

16.1.2 DISPLAY RAM

The Display RAM (Block 0 only) is initialised on power-up to a value of 20H. The contents of the Display RAM are maintained when entering Idle mode. If Idle mode is exited using an interrupt then the contents are unchanged, if Idle mode is exited using a reset then the contents are re-initialised to 20H.

16.2 Memory mapping

The dedicated Auxiliary RAM area occupies 0.75 kbytes, with an address range from 0000H to 0300H. The Display RAM occupies 1.25 kbytes with an address range from 2000H to 24FFH for TXT mode and 8000H to 84FFH for CC mode. The two modes although having different address ranges occupy the same physical DRAM area.

16.3 Addressing memory

The memory can be addressed by the microcontroller in two ways, either directly using a MOVX command, or via Special Function Registers depending on what address is required.

The dedicated Auxiliary RAM, and Display memory in the range 8000H to 86FFH, can only be accessed using the MOVX command.

The Display memory in the range 2000H to 23FFH can either be directly accessed using the MOVX, or via the Special Function Registers.

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16.3.1 TXT DISPLAY MEMORY SFR ACCESS

The Display memory when in TXT mode (see Fig.14) is configured as 40 columns wide by 25 rows and occupies 1K x 8 bits of memory. The row and column is selected using TXT9.R<4:0> and TXT10.C<5:0>. The data at the selected position can be read or written using TXT11.D<7:0>.

Whenever a read or write is performed on TXT11, the row values stored in TXT9 and column value stored in TXT10 are automatically incremented. For rows 0 to 24 the column value is incremented up to a maximum of 39, at which point it resets to a logic 0 and increments the row counter value. When row 25 column 23 is reached the values of the row and column are both reset to logic 0.

Writing values outside of the valid range for TXT9 or TXT10 will cause undetermined operation of the auto-incrementing function for accesses to TXT11.

16.3.2 TXT DISPLAY MEMORY MOVX ACCESS

It is important for the generation of OSD displays, that use this mode of access, to understand the mapping of the MOVX address onto the display row and column value. This mapping of row and column onto address is shown in Table 10. The values shown are added onto a base address for the required memory block (see Fig.13) to give a 16-bit address.

16.4 Page clearing

Page clearing is performed on request from the microcontroller under the control of the embedded software.

At power-on and reset the Text Display memory (from 2000H to 23FFH) is cleared to the value of 20H. The TXT13.PAGE CLEARING bit will be set while this takes place.

16.4.1 DATA CAPTURE PAGE CLEAR

Not present in the SAA55xx OSD only devices.

16.4.2 SOFTWARE PAGE CLEAR

The software can also initiate a page clear, by setting the TXT9.CLEAR MEMORY bit. The CLEAR MEMORY bit is not latched so the software does not have to reset it after it has been set.

Only one page can be cleared in a TV line so if the software requests a page clear it will be carried out on the next TV line on which the Data Capture hardware does not force the page to be cleared. A flag, TXT13.PAGE CLEARING, is provided to indicate that a software requested page clear is being carried out. The flag is set when a logic 1 is written into the TXT9.CLEAR MEMORY bit and is reset when the page clear has been completed.

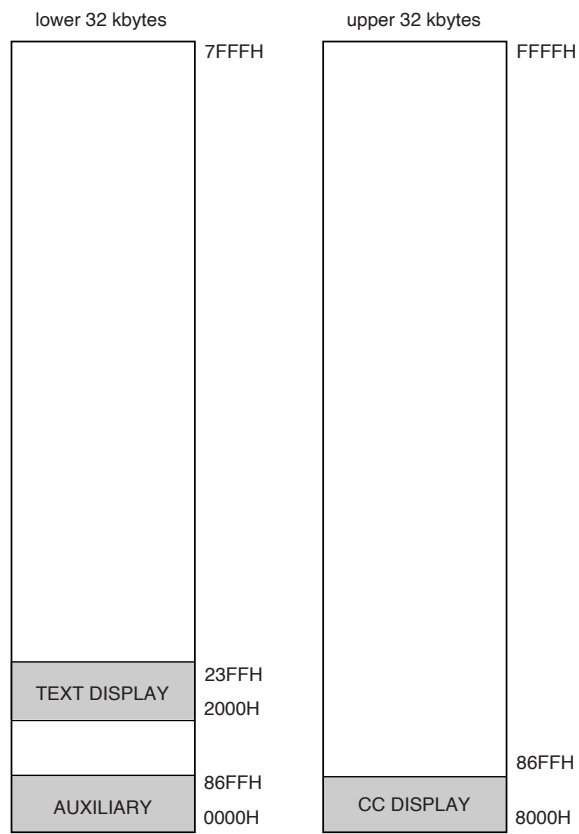
Inventory page clearing is not present in the SAA55xx OSD only devices.

Table 10 Column and row to MOVX address (lower 10 bits of address)

| ROW | COL.0 | ... | COL.23 | ... | COL.31 | COL.32 | ... | COL.39 |
|--------|-------|-----|--------|-----|--------|--------|-----|--------|
| Row 0 | 000H | ... | 017H | ... | 01FH | 3F8H | ... | 3FFH |
| Row 1 | 020H | ... | 037H | ... | 03FH | 3F0H | ... | 3F7H |
| ... | ... | ... | ... | ... | ... | ... | ... | ... |
| Row 23 | 2E0H | ... | 3F7H | ... | 2FFH | 340H | ... | 347H |
| Row 24 | 300H | ... | 317H | ... | 31FH | 338H | ... | 33FH |
| Row 25 | 320H | ... | 337H | ... | | | ... | |

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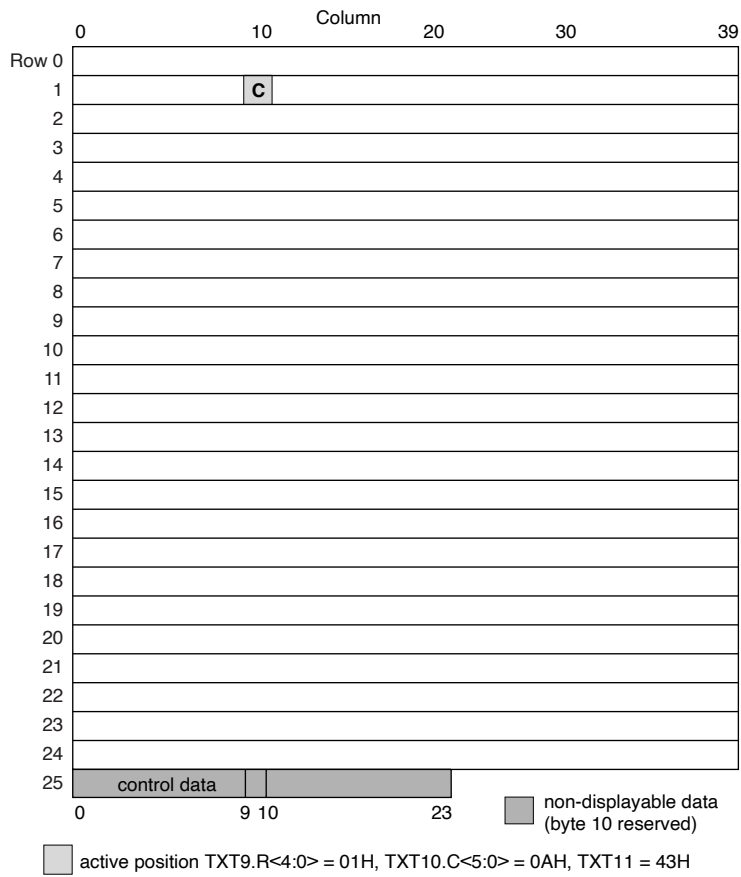


GSA011

Fig.13 DRAM memory mapping.

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MBK962

Fig.14 TXT memory map.

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17 DATA CAPTURE

The Data Capture section takes in the analog Composite Video and Blanking Signal (CVBS), and from this extracts the required data, which is then decoded and stored in memory.

The extraction of the data is performed in the digital domain. The first stage is to convert the analog CVBS signal into a digital form. This is done using an ADC sampling at 12 MHz. The data and clock recovery is then performed by a Multi-Rate Video Input Processor (MuVIP). From the recovered data and clock, the serial Closed Captioning data is converted to parallel and stored as two bytes per line. The extracted data is stored in SFR locations.

17.1 Data Capture features

- Two CVBS inputs
- Data Capture for Line 21 Data Service
- Video Signal Quality Detector.

17.1.1 CVBS SWITCH

The CVBS switch is used to select the required analog input depending on the value of TXT8.CVBS1/CVBS0.

17.1.2 ANALOG-TO-DIGITAL CONVERTER

The output of the CVBS switch is passed to a differential to single ended converter, although in this device it is used in single ended configuration with a reference. The analog output of the differential to single ended converter is converted into a digital representation by a full-flash ADC with a sampling rate of 12 MHz.

17.1.3 MULTI-RATE VIDEO INPUT PROCESSOR

The multi-rate video input processor is a Digital Signal Processor designed to extract the data and recover the clock from a digitized CVBS signal. The only data and clock standard that can be recovered in the OSD only devices is Closed Caption at a data rate of approximately 503.5 kHz.

17.1.4 DATA CAPTURE TIMING

The Data Capture timing section uses the synchronisation information extracted from the CVBS signal to generate the required horizontal and vertical reference timings.

The timing section automatically recognizes and selects the appropriate timings for either 625 (50 Hz) synchronisation or 525 (60 Hz) synchronisation.

A flag TXT12.VIDEO SIGNAL QUALITY is set when the timing section is locked correctly to the incoming CVBS signal. When TXT12.VIDEO SIGNAL QUALITY is set another flag TXT12.525/625 SYNC can be used to identify the standard.

17.1.5 LINE 21 DATA SERVICES

The Line 21 Data Services is transmitted on line 21 of a 525-line broadcast system and is used for Captioning information, Text information and Extended Data Services. Full Details can be found in "*Recommended Practise for Line 21 Data Service EIA-608*".

Closed Caption Line 21 data is only acquired when TXT21.CC ON bit is set.

Two bytes of data are stored per field in SFRs, the first byte is stored in CCDAT1 and the second byte is stored in CCDAT2. The contents of each CCDAT register are reset to 00H at the start of the Closed Caption line defined by CCLIN.CS<4:0>. At the end of the Closed Caption line an interrupt is generated if IE.ECC is active.

The processing of the Closed Caption data to convert into a displayable format is performed by software.

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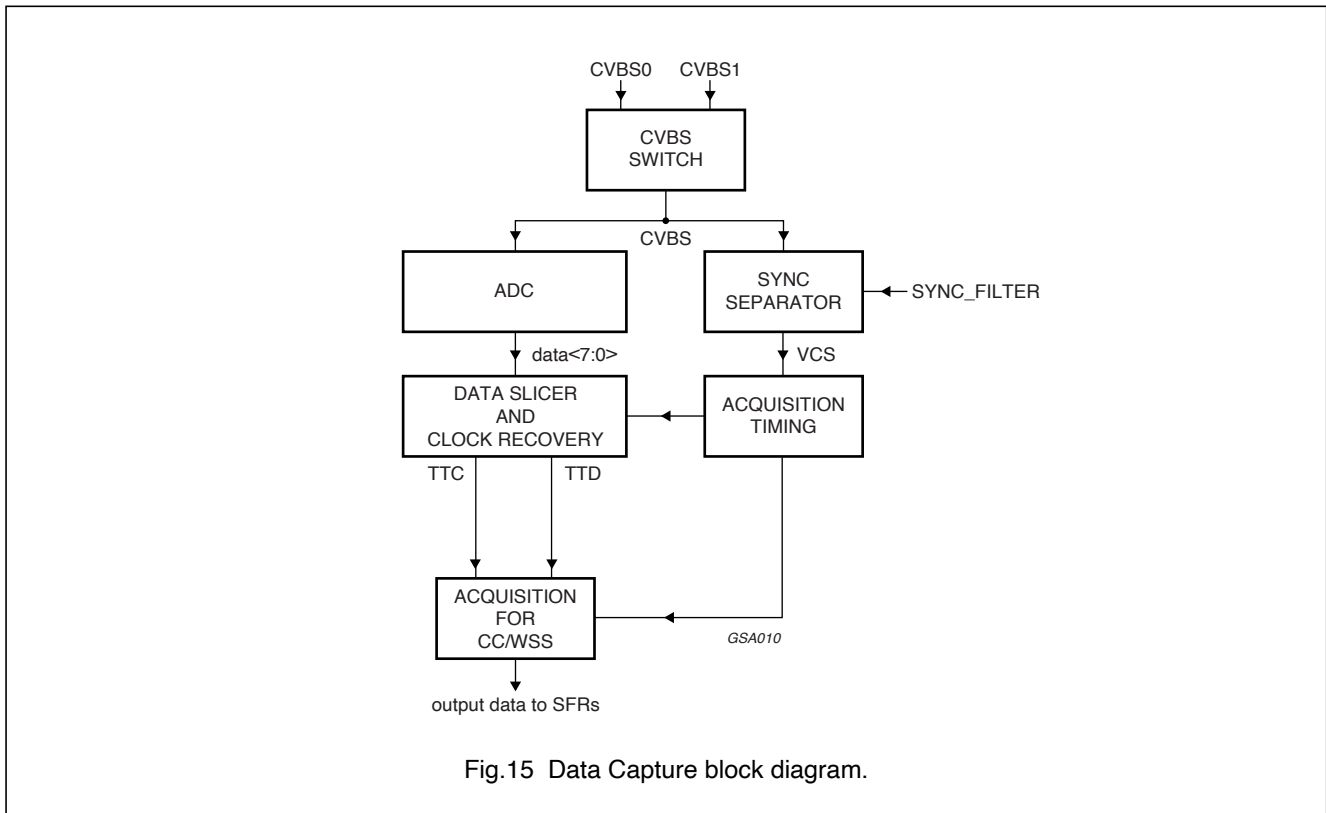


Fig.15 Data Capture block diagram.

18 DISPLAY

The display section is based on the requirements for US Closed Caption. There are some enhancements for use with locally generated On-Screen Displays.

The display section reads the contents of the Display memory and interprets the control/character codes. From this information and other global settings, the display produces the required RGB signals and video/data (Fast Blanking) signal for a TV signal processing device.

The display is synchronised to the TV signal processing device by way of horizontal and vertical sync signals provided by external circuits (Slave Sync mode). From these signals all display timings are derived.

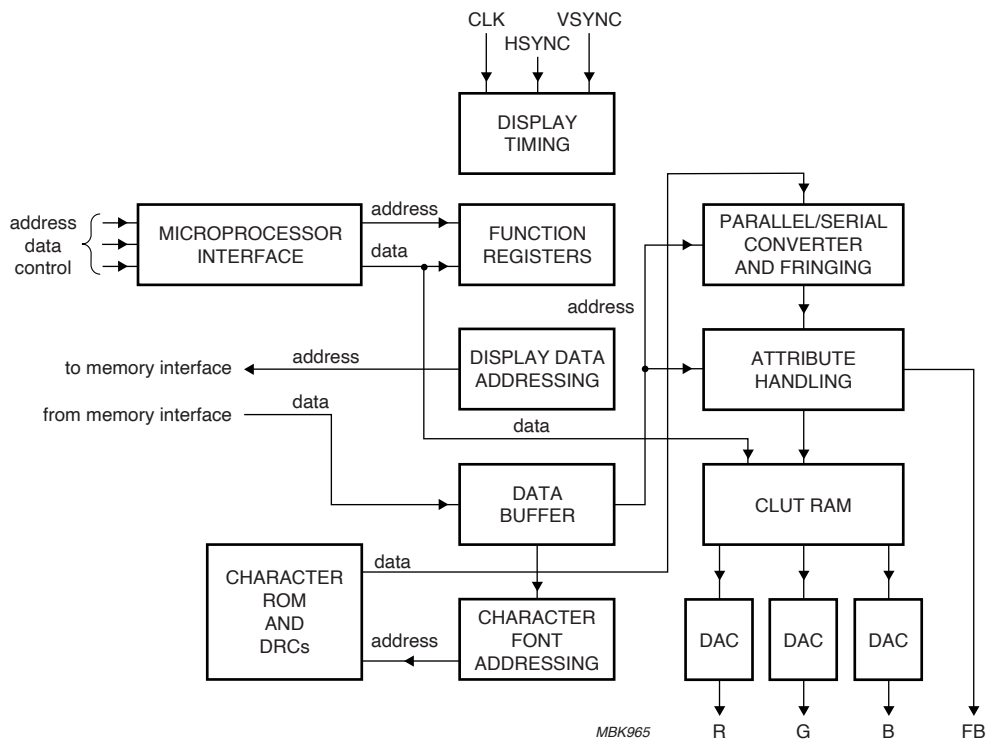
18.1 Display features

- Teletext style OSD and Enhanced OSD modes
- US Closed Caption features
- Serial and Parallel display attributes
- Single/double/quadruple width and height for characters
- Scrolling of display region
- Variable flash rate controlled by software

- Globally selectable scan lines per row 9, 10, 13 or 16
- Globally selectable character matrix (H x V) 12 x 9, 12 x 10, 12 x 13 or 12 x 16
- Italics
- Soft colours using CLUT with 4096 colour palette
- Underline
- Overline
- Fringing (shadow) selectable from N-S-E-W direction
- Fringe colour selectable
- Meshing of defined area
- Contrast reduction of defined area
- Cursor
- Special Graphics characters with two planes, allowing four colours per character
- 32 software redefinable On-Screen Display characters
- 4 WST character sets (G0/G2) in single device (e.g. Latin, Cyrillic, Greek, Arabic)
- G1 Mosaic graphics, Limited G3 Line drawing characters
- WST character sets and Closed (including extended) Caption character set in a single device.

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Fig.16 Display block diagram.

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18.2 Display modes

The display section has two distinct modes with different features available in each. The two modes are:

- **TXT:** This is the display configured for WST with additional serial and global attributes. The display is configured as a fixed 25 rows with 40 characters per row. In the OSD only family this mode can only be utilised for display of Text style OSD, no Teletext Data Capture is present.
- **CC:** This is the display configured as the US Closed Caption mode. The display is configured as a maximum of 16 rows with a maximum of 48 characters per row.

In both of the above modes the character matrix, and TV lines per row can be defined. There is an option of 9, 10, 13 and 16 TV lines per display row, and a character matrix (H x V) of 12 x 9, 12 x 10, 12 x 13 or 12 x 16. Not all combinations of TV lines per row and maximum display rows give a sensible OSD display, since there is a limited number of TV scan lines available.

Special Function Register TXT21 and memory mapped registers are used to control the mode selection.

18.3 Display feature descriptions

All display features are now described in detail for both TXT and CC modes.

18.3.1 FLASH

Flashing causes the foreground colour pixel to be displayed as the background pixels. The flash frequency is controlled by software setting and resetting the MMR Status (see Table 28) at the appropriate interval.

CC: This attribute is valid from the time set (see Table 16) until the end of the row or until otherwise modified.

TXT: This attribute is set by the control character 'flash' (08H) and remains valid until the end of the row or until reset by the control character 'steady' (09H).

18.3.2 BOXES

CC: This attribute is valid from the time set until end of row or otherwise modified if set with Serial Mode 0. If set with Serial Mode 1, then it is set from the next character onwards.

In Text mode (within CC mode) the background colour is displayed regardless of the setting of the box attribute bit. Boxes take effect only during mixed mode, where boxes are set in this mode the background colour is displayed. Character locations where boxes are not set show video/screen colour (depending on the setting in the MMR Display Control) instead of the background colour.

TXT: Two types of boxes exist, the teletext box and the OSD box. The teletext box is activated by the 'start box' control character (0BH). Two start box characters are required to begin a teletext box, with the box starting between the 2 characters. The box ends at the end of the line or after a 'end box' control character.

TXT mode can also use OSD boxes, they are started using size, implying OSD control characters (BCH, BDH, BEH and BFH). The box starts after the control character (set after) and ends either at the end of the row or at the next size implying OSD character (set at).

The attributes flash, teletext box, conceal, separate graphics, twist and hold graphics are all reset at the start of an OSD box, as they are at the start of the row. OSD boxes are only valid in TV mode which is defined by TXT5 = 03H and TXT6 = 03H.

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18.3.3 SIZE

The size of the characters can be modified in both the horizontal and vertical directions.

CC: Two sizes are available in both the horizontal and vertical directions. The sizes available are normal (x1), double (x2) height/width and any combination of these. The attribute setting is always valid for the whole row. Mixing of sizes within a row is not possible.

TXT: Three horizontal sizes are available normal (x1), double (x2) and quadruple (x4). The control characters 'normal size' (0CH/BCH) enables normal size, the 'double width' or 'double size' (0EH/BEH/0FH/BFH) enables double width characters.

Any two consecutive combination of 'double width' or 'double size' (0EH/BEH/0FH/BFH) activates quadruple width characters, provided quadruple width characters are enabled by TXT4.QUAD WIDTH ENABLE.

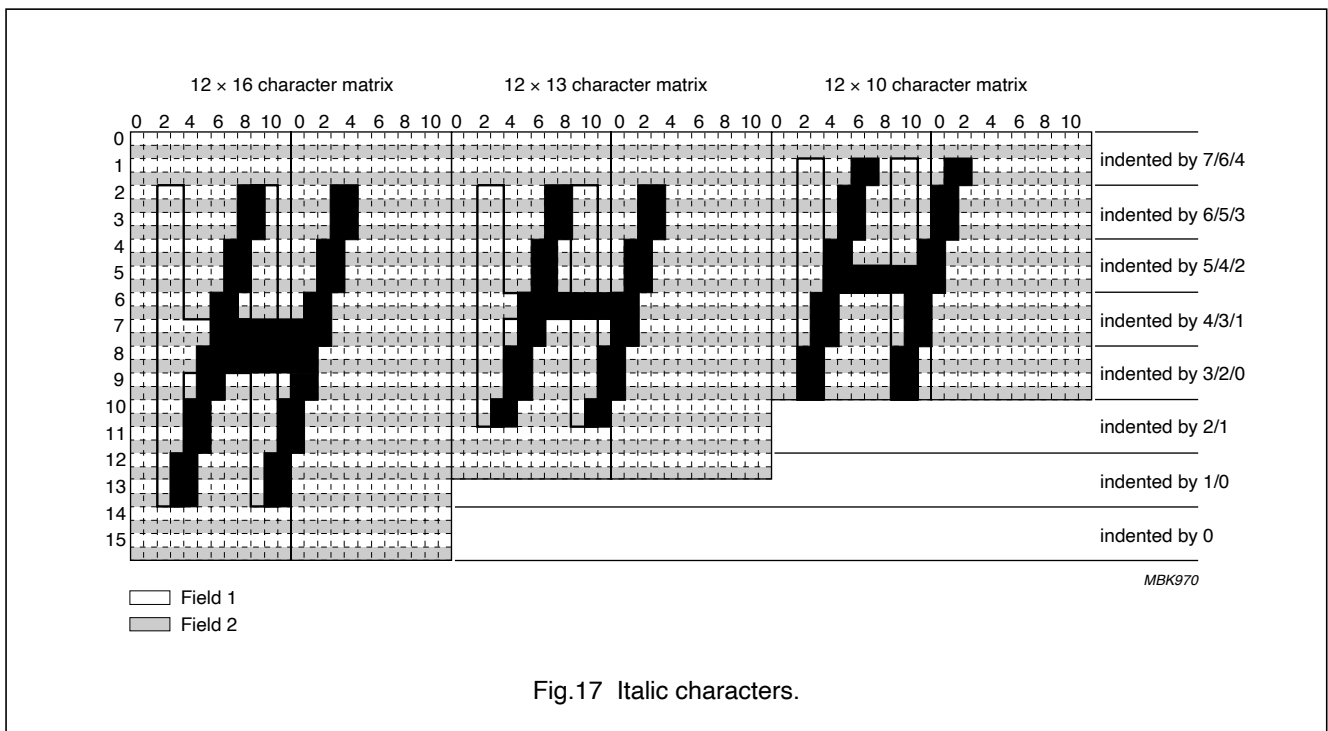
Three vertical sizes are available normal (x1), double (x2) and quadruple (x4). The control characters 'normal size' (0CH/BCH) enable normal size, the 'double height' or 'double size' (0DH/BDH/0FH/BFH) enable double height characters. Quadruple height characters are achieved by using double height characters and setting the global attributes TXT7.DOUBLE HEIGHT (expand) and TXT7.BOTTOM/TOP.

If double height characters are used in Teletext mode, single height characters in the lower row of the double height character are automatically disabled.

18.3.4 ITALIC

CC: This attribute is valid from the time set until the end of the row or otherwise modified. The attribute causes the character foreground pixels to be offset horizontally by 1 pixel per 4 scan lines (interlaced mode). The base is the bottom left character matrix pixel. The pattern of the character is indented as shown in Fig.17.

TXT: The Italic attribute is not available.



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18.3.5 COLOURS

A CLUT (Colour Look-Up Table) with 16 colour entries is provided. The colours are programmable out of a palette of 4096 (4 bits per R, G and B). The CLUT is defined by writing data to a RAM that resides in the MOVX address space of the 80C51.

Table 11 CLUT colour values

| RED<3:0> (B11 TO B8) | GREEN<3:0> >(B7 TO B4) | BLUE<3:0> (B3 TO B0) | COLOUR ENTRY |
|-------------------------|---------------------------|-------------------------|-----------------|
| 0000 | 0000 | 0000 | 0 |
| 0000 | 0000 | 1111 | 1 |
| | | | .. |
| 1111 | 1111 | 0000 | 14 |
| 1111 | 1111 | 1111 | 15 |

18.3.6 FOREGROUND COLOUR

CC: The foreground colour can be chosen from 8 colours on a character-by-character basis. Two sets of 8 colours are provided. A serial attribute switches between the banks (see Table 16, Serial Mode 1, bit 7). The colours are the CLUT entries 0 to 7 or 8 to 15.

TXT: The foreground colour is selected via a control character (see Table 16). The colour control characters take effect at the start of the next character (set-after) and remain valid until the end of the row, or until modified by a control character. Only 8 foreground colours are available.

The text foreground control characters map to the CLUT entries is shown in Table 12.

Table 12 Foreground CLUT mapping

| CONTROL CODE | DEFINED COLOUR | CLUT ENTRY |
|-----------------|-------------------|------------|
| 00H | black | 0 |
| 01H | red | 1 |
| 02H | green | 2 |
| 03H | yellow | 3 |
| 04H | blue | 4 |
| 05H | magenta | 5 |
| 06H | cyan | 6 |
| 07H | white | 7 |

18.3.7 BACKGROUND COLOUR

CC: This attribute is valid from the time set until end of row or otherwise modified if set with Serial Mode 0. If set with Serial Mode 1, then the colour is set from the next character onwards.

The background colour can be chosen from all 16 CLUT entries.

TXT: The control character 'new background' (1DH) is used to change the background colour to the current foreground colour. The selection is immediate (set at) and remains valid until the end of the row or until otherwise modified.

The Text background control characters map to the CLUT entries as shown in Table 13.

Table 13 Background CLUT mapping

| CONTROL CODE | DEFINED COLOUR | CLUT ENTRY |
|-----------------|-------------------|------------|
| 00H + 1DH | black | 8 |
| 01H + 1DH | red | 9 |
| 02H + 1DH | green | 10 |
| 03H + 1DH | yellow | 11 |
| 04H + 1DH | blue | 12 |
| 05H + 1DH | magenta | 13 |
| 06H + 1DH | cyan | 14 |
| 07H + 1DH | white | 15 |

18.3.8 BACKGROUND DURATION

The attribute when set takes effect from the current position until the end of the text display defined in the MMR Text Area End.

CC: The background duration attribute (see Table 16, Serial Mode 1, bit 8) in combination with the End Of Row attribute (see Table 16, Serial Mode 1, bit 9) forces the background colour to be displayed on the row until the end of the text area is reached.

TXT: This attribute is not available.

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18.3.9 UNDERLINE

The underline attribute causes the characters to have the bottom scan line of the character cell forced to foreground colour, including spaces. If background duration is set, then underline is set until the end of the text area.

CC: The underline attribute (see Table 16, Serial Mode 0/1, bit 4) is valid from the time set until the end of row or otherwise modified.

TXT: This attribute is not available.

18.3.10 OVERLINE

The overline attribute causes the characters to have the top scan line of the character cell forced to foreground colour, including spaces. If background duration is set, then overline is set until the end of the text area.

CC: The overline attribute (see Table 16, Serial Mode 0/1, bit 5) is valid from the time set until end of row or otherwise modified. Overlining of italic characters is not possible.

TXT: This attribute is not available.

18.3.11 END OF ROW

CC: The number of characters in a row is flexible and can be determined by the end of row attribute (see Table 16, Serial Mode 1, bit 9). However, the maximum number of character positions displayed is determined by the setting of the MMR Text Position Horizontal and MMR Text Area End.

Note that when using the end of row attribute the next character location after the attribute should always be occupied by a 'space'.

TXT: This attribute is not available, row length is fixed at 40 characters.

18.3.12 FRINGING

A fringe (shadow) can be defined around characters. The fringe direction is individually selectable in any of the North, South, East and West direction using the MMR Fringing Control. The colour of the fringe can also be defined as one of the entries in the CLUT, again using MMR Fringing Control. An example of south and south-west fringing is shown in Fig.18.

CC: The fringe attribute (see Table 16, Serial Mode 0, bit 9) is valid from the time set until the end of the row or otherwise modified.

TXT: The display of fringing in TXT mode is controlled by the TXT4.SHADOW ENABLE bit.

When set, all the alphanumeric characters being displayed are shadowed, graphics characters are not shadowed.

18.3.13 MESHING

The attribute effects the background colour being displayed. Alternate pixels are displayed as the background colour or video. The structure is offset by 1 pixel from scan line to scan line, thus achieving a checker board display of the background colour and video. An example of meshing is shown in Fig.19.

CC: The setting of the MSH bit in MMR Display Control has the effect of meshing any background colour.

TXT: There are two meshing attributes one that only affects black background colours TXT4.B MESH ENABLE and a second that only affects backgrounds other than black TXT4.C MESH ENABLE. A black background is defined as CLUT entry 8, a non-black background is defined as CLUT entry 9 to 15.

18.3.14 CURSOR

The cursor operates by reversing the background and foreground colours in the character position pointed to by the active cursor position. The cursor is enabled using TXT7.CURSOR ON. When active, the row the cursor appears on is defined by TXT9.R<4:0> and the column is defined by TXT10.C<5:0>. The position of the cursor can be fixed using TXT9.CURSOR FREEZE. The cursor display is shown in Fig.20.

CC: The valid range for row is 0 to 15. The valid range for column is 0 to 47. The cursor remains rectangular at all times, its shape is not affected by italic attribute, therefore it is not advised to use the cursor with italic characters.

TXT: The valid range for row positioning is 0 to 24. The valid range for column is 0 to 39.

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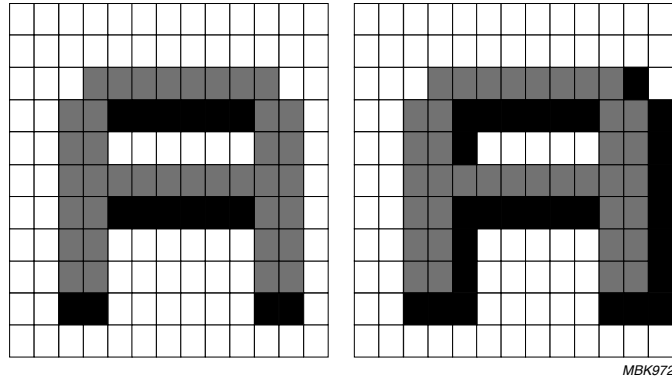


Fig.18 South and south-west fringing.

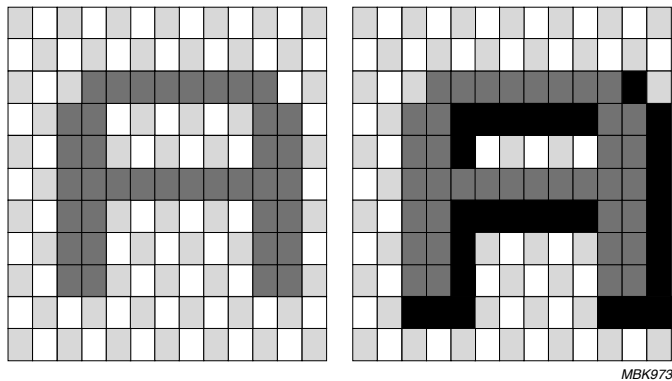


Fig.19 Meshing and Meshing/fringing (south + west).



Fig.20 Cursor display.

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18.3.15 SPECIAL GRAPHICS CHARACTERS

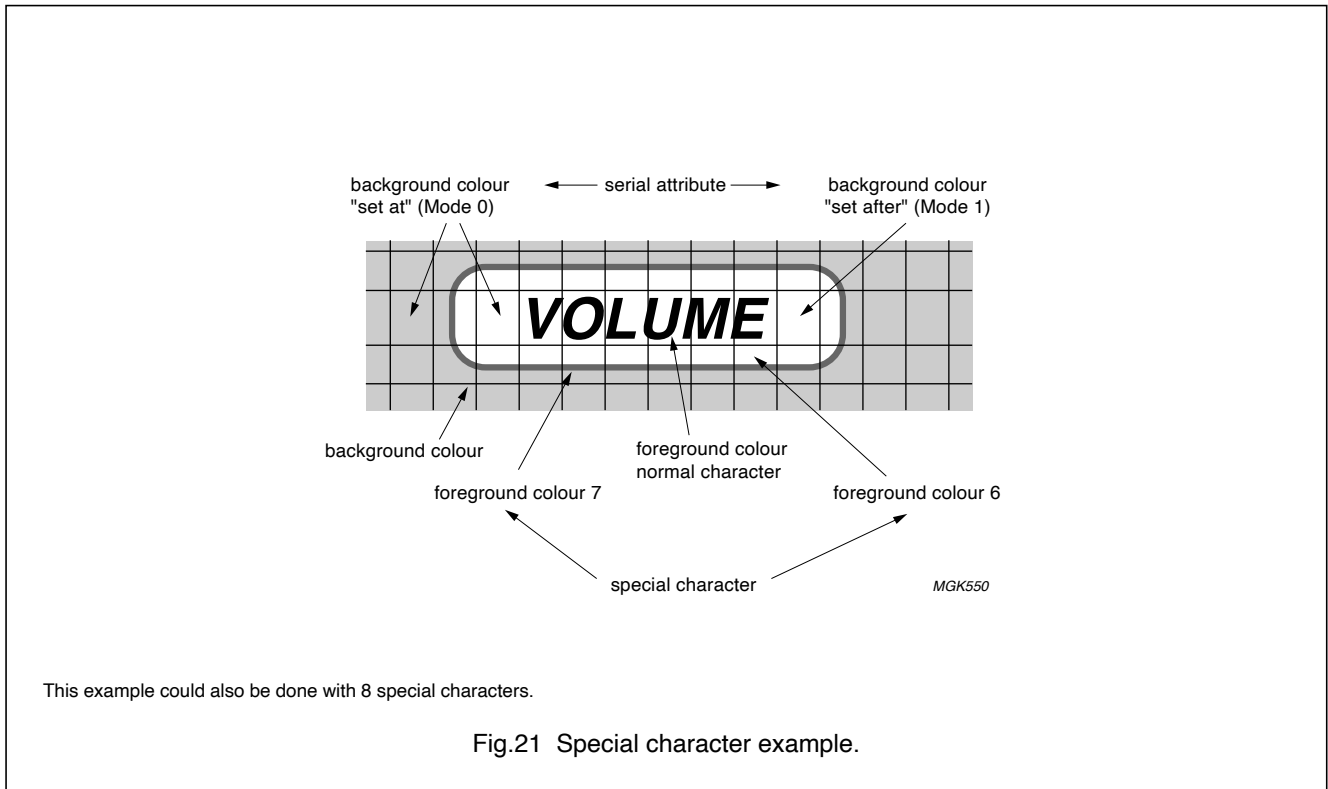
CC/TXT: Several special characters are provided for improved OSD effects. These characters provide a choice of four colours within a character cell. The total number of special graphics characters is limited to 16. They are stored in the character codes 8XH and 9XH of the character table (32 ROM characters), or in the DRCs which overlay character codes 8XH and 9XH. Each special graphics character uses two consecutive normal characters.

Fringing, underline and overline is not possible for special graphics characters. Special graphics characters are activated when `TXT20.OSD PLANES = 1`.

Table 14 Special character colour allocation

| PLANE 1 | PLANE 0 | COLOUR ALLOCATION |
|---------|---------|-------------------|
| 0 | 0 | background colour |
| 0 | 1 | foreground colour |
| 1 | 0 | CLUT entry 6 |
| 1 | 1 | CLUT entry 7 |

If the screen colour is transparent (implicit in mixed mode) and inside the object the box attribute is set, then the object is surrounded by video. If the box attribute is not set the background colour inside the object will also be displayed as transparent.



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18.4 Character and attribute coding

This section describes the character and attribute coding for each mode.

18.4.1 CC MODE

Character coding is split into character oriented attributes (parallel) and character group coding (serial). The serial attributes take effect either at the position of the attribute (set at), or at the following location (set after) and remain effective until either modified by a new serial attribute or until the end of the row. A serial attribute is represented as a space (the space character itself however is not used for this purpose), the attributes that are still active, e.g. overline and underline will be visible during the display of the space.

The default setting at the start of a row is:

- ×1 size
- Flash off
- Overline off
- Underline off
- Italics off
- Display mode = superimpose
- Fringing off
- Background colour duration = 0
- End of row = 0.

The coding is done in 12-bit words. The codes are stored sequentially in the Display memory. A maximum of 768 character positions can be defined for a single display.

Table 15 Parallel character coding

| BITS | DESCRIPTION |
|---------|---------------------------------|
| 0 to 7 | 8 bit character code |
| 8 to 10 | 3 bits for 8 foreground colours |
| 11 | mode bit: 0 = Parallel code |

18.4.2 TXT MODE

Character coding is in a serial format, with only one attribute being changed at any single location. The serial attributes take effect either at the position of the attribute (set at), or at the following location (set after). The attribute remains effective until either modified by new serial attributes or until the end of the row.

The default settings at the start of a row are:

- Foreground colour white (CLUT address 7)
- Background colour black (CLUT address 8)
- Horizontal size ×1, vertical size ×1 (normal size)
- Alphanumeric on
- Contiguous mosaic graphics
- Release mosaics
- Flash off
- Box off
- Conceal off
- Twist off.

The attributes have individual codes which are defined in the basic character table (see Fig.22).

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Table 16 Serial character coding

| BIT | DESCRIPTION | | |
|--------|--|--|--|
| | SERIAL MODE 0 (SET AT) | SERIAL MODE 1 | |
| | | CHAR.POS. 1 (SET AT) | CHAR.POS. >1 (SET AFTER) |
| 0 to 3 | 4 bits for 16 background colours | 4 bits for 16 background colours | 4 bits for 16 background colours |
| 4 | Underline switch: 0 = underline off 1 = underline on | Horizontal size: 0 = normal 1 = x2 | Underline switch: 0 = underline off 1 = underline on |
| 5 | Overline switch: 0 = overline off 1 = overline on | Vertical size: 0 = normal 1 = x2 | Overline switch: 0 = overline off 1 = overline on |
| 6 | Display mode: 0 = superimpose 1 = boxing | Display mode: 0 = superimpose 1 = boxing | Display mode: 0 = superimpose 1 = boxing |
| 7 | Flash switch: 0 = flash off 1 = flash on | Foreground colour switch: 0 = Bank 0 (colours 0 to 7) 1 = Bank 1 (colours 8 to 15) | Foreground colour switch: 0 = Bank 0 (colours 0 to 7) 1 = Bank 1 (colours 8 to 15) |
| 8 | Italics switch 0 = italics off 1 = italics on | Background colour duration: 0 = stop BGC 1 = set BGC to end of row | Background colour duration (set at): 0 = stop BGC 1 = set BGC to end of row |
| 9 | Fringing switch: 0 = fringing off 1 = fringing on | End of row: 0 = continue row 1 = end row | End of row (set at): 0 = continue row 1 = end row |
| 10 | Switch for serial coding: 0 = mode 0 1 = mode 1 | Switch for serial coding: 0 = mode 0 1 = mode 1 | Switch for serial coding 0 = mode 0 1 = mode 1 |
| 11 | Mode bit: 1 = serial code | Mode bit: 1 = serial code | Mode bit: 1 = serial code |

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| E/W = 0 | | | E/W = 1 | | |
|---------|---|---|---------|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| D | E | F | D | E | F |
| 0 | 1 | 2 | 0 | 1 | 2 |
| 3 | 4 | 5 | 3 | 4 | 5 |
| 6 | 7 | 8 | 6 | 7 | 8 |
| 9 | A | B | 9 | A | B |
| C | D | E | C | D | E |
| F | G | H | F | G | H |
| I | J | K | I | J | K |
| L | M | N | L | M | N |
| O | P | Q | O | P | Q |
| R | S | T | R | S | T |
| U | V | W | U | V | W |
| X | Y | Z | X | Y | Z |
| [|] | ~ | [|] | ~ |

| BIT S | b_7 | b_6 | b_5 | b_4 | column | 0 | 1 | 2 | 2a | 3 | 3a | 4 | 5 | 6 | 6a | 7 | 7a | 8 | 8a | 9 | 9a | A | B | C | |
|-------|-------|-------|-------|-------|--------|---------------|---------------------|---------|----|---------|---------|---------|---------|---------|----|---|-----|-----|-----|-----|-----|-----|---------------------|-------------------|---|
| 0 | 0 | 0 | 0 | 0 | 0 | alpha black | graphics black | | | 0 | | nat opt | P | nat opt | p | | OSD | OSD | OSD | OSD | OSD | OSD | # | back-ground black | U |
| 0 | 0 | 0 | 1 | 1 | 1 | alpha red | graphics red | ! | 1 | A | Q | a | q | | | | OSD | OSD | OSD | OSD | OSD | \$ | back-ground red | A | |
| 0 | 0 | 1 | 0 | 2 | 2 | alpha green | graphics green | 2 | B | R | b | r | | | | | OSD | OSD | OSD | OSD | OSD | X | back-ground green | E | |
| 0 | 0 | 1 | 1 | 3 | 3 | alpha yellow | graphics yellow | nat opt | 3 | C | S | s | | | | | OSD | OSD | OSD | OSD | OSD | 2 | back-ground yellow | I | |
| 0 | 1 | 0 | 0 | 4 | 4 | alpha blue | graphics blue | nat opt | 4 | D | T | t | | | | | OSD | OSD | OSD | OSD | OSD | ä | back-ground blue | ö | |
| 0 | 1 | 0 | 1 | 5 | 5 | alpha magenta | graphics magenta | % | 5 | E | U | e | u | | | | OSD | OSD | OSD | OSD | OSD | ë | back-ground magenta | ü | |
| 0 | 1 | 1 | 0 | 6 | 6 | alpha cyan | graphics cyan | & | 6 | F | V | f | v | | | | OSD | OSD | OSD | OSD | OSD | ö | back-ground cyan | ö | |
| 0 | 1 | 1 | 1 | 7 | 7 | alpha white | graphics white | ' | 7 | G | W | w | | | | | OSD | OSD | OSD | OSD | OSD | ü | back-ground white | ü | |
| 1 | 0 | 0 | 0 | 8 | 8 | flash | conceal display | C | 8 | H | X | h | x | | | | OSD | OSD | OSD | OSD | OSD | Ä | ö | S | |
| 1 | 0 | 0 | 1 | 9 | 9 | steady | contiguous graphics |) | 9 | I | Y | i | y | | | | OSD | OSD | OSD | OSD | OSD | È | Ü | ä | |
| 1 | 0 | 1 | 0 | A | A | end box | separated graphics | * | I | J | Z | j | z | | | | OSD | OSD | OSD | OSD | OSD | Ö | ö | ï | |
| 1 | 0 | 1 | 1 | B | B | start box | twist | + | I | K | nat opt | k | nat opt | | | | OSD | OSD | OSD | OSD | OSD | Ü | ü | ö | |
| 1 | 1 | 0 | 0 | C | C | normal height | black back-ground | , | L | nat opt | l | nat opt | | | | | OSD | OSD | OSD | OSD | OSD | ä | normal size OSD | Ä | |
| 1 | 1 | 0 | 1 | D | D | double height | new back-ground | - | M | nat opt | m | nat opt | | | | | OSD | OSD | OSD | OSD | OSD | é | double height OSD | é | |
| 1 | 1 | 1 | 0 | E | E | double width | hold graphics | . | N | nat opt | n | nat opt | | | | | OSD | OSD | OSD | OSD | OSD | í | double width OSD | í | |
| 1 | 1 | 1 | 1 | F | F | double size | release graphics | / | O | nat opt | o | nat opt | | | | | OSD | OSD | OSD | OSD | OSD | ó | double size OSD | ó | |

nat opt character dependent on the language of page, refer to National Option characters
 OSD customer definable On-Screen Display character

Fig.22 TXT basic character set (Pan-European).

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18.5 Screen and global controls

A number of attributes are available that affect the whole display region, and cannot be applied selectively to regions of the display.

18.5.1 TV SCAN LINES PER ROW

The number of TV scan lines per field used for each display row can be defined, the value is independent of the character size being used. The number of lines can be either 10, 13 or 16 per display row. The number of TV scan lines per row is defined `TXT21.DISPLAY LINES<1:0>`.

A value of 9 lines per row can be achieved if the display is forced into 525-line display mode by `TXT17.FORCE DISP<1:0>`, or if the device is in 10 line mode and the automatic detection circuitry within display finds 525-line display syncs.

18.5.2 CHARACTER MATRIX (H x V)

There are three different character matrices available, these are 12 x 10, 12 x 13 and 12 x 16. The selection is made using `TXT21.CHAR SIZE<1:0>` and is independent of the number of display lines per row.

If the character matrix is less than the number of TV scan lines per row then the matrix is padded with blank lines. If the character matrix is greater than the number of TV scan lines then the character is truncated.

18.5.3 DISPLAY MODES

CC: When attributes superimpose or boxing (see Table 16, Serial Mode 0/1, bit 6) are set, the resulting display depends on the setting of the following screen control mode bits in the MMR Display Control.

TXT: The display mode is controlled by the bits in the `TXT5` and `TXT6` registers. There are three control functions - Text on, Background on and Picture on. Separate sets of bits are used inside and outside teletext boxes so that different display modes can be invoked. `TXT6` is used if the newsflash (C5) or subtitle (C6) bits in row 25 of the basic page memory are set otherwise `TXT5` is used. This allows the software to set up the type of display required on newsflash and subtitle pages (e.g. text inside boxes, TV picture outside) this will be invoked without any further software intervention when such a page is acquired.

When teletext box control characters are present in the display page memory, the appropriate box control bit must be set, `TXT7.BOX ON 0`, `TXT7.BOX ON 1 – 23` or `TXT7.BOX ON 24`. This allows the display mode to be different inside the teletext box compared to outside. These bits are present to allow boxes in certain areas of the screen to be disabled. The use of teletext boxes for OSD messages has been superseded in this device by the OSD box concept, but these bits remain to allow teletext boxes to be used, if required.

Table 17 Display modes

| MOD 0 | MOD 1 | DISPLAY MODE | DESCRIPTION |
|-------|-------|---------------------|--|
| 0 | 0 | Video | Disables all display activities, sets the RGB to true black and VDS to video. |
| 1 | 0 | Full Text | Displays screen colour at all locations not covered by character foreground or background colour. The box attribute has no effect. |
| 0 | 1 | Mixed Screen Colour | Displays screen colour at all locations not covered by character foreground, within boxed areas or, background colour. |
| 1 | 1 | Mixed Video | Mixed Video mode displays video at all locations not covered by character foreground, within boxed areas or, background colour. |

Table 18 TXT display control bits

| PICTURE ON | TEXT ON | BACKGROUND ON | EFFECT |
|------------|---------|---------------|---|
| 0 | 0 | X | Text mode, black screen |
| 0 | 1 | 0 | Text mode, background always black |
| 0 | 1 | 1 | Text mode |
| 1 | 0 | X | Video mode |
| 1 | 1 | 0 | Mixed text and TV mode |
| 1 | 1 | 1 | Text mode, TV picture outside text area |

18.5.4 SCREEN COLOUR

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Screen colour is displayed from 10.5 ms to 62.5 ms after the active edge of the HSYNC input and on TV lines 23 to 310 inclusive, for a 625-line display, and lines 17 to 260 inclusive for a 525-line display.

CC: The screen colour is defined by the MMR Display Control and points to a location in the CLUT table. The screen colour covers the full video width. It is visible when the Full Text or Mixed Screen Colour mode is set and no foreground or background pixels are being displayed.

TXT: The register bits TXT17.SCREEN COL<2:0> can be used to define a colour to be displayed in place of TV picture and the black background colour. If the bits are all set to zero, the screen colour is defined as 'transparent' and TV picture and background colour are displayed as normal. Otherwise the bits define CLUT entries 9 to 15.

18.6 Text display controls

18.6.1 TEXT DISPLAY CONFIGURATION (CC MODE)

Two types of areas are possible. The one area is static and the other is dynamic. The dynamic area allows scrolling of a region to take place. The areas cannot cross each other. Only one scroll region is possible.

18.6.2 DISPLAY MAP

The display map allows a flexible allocation of data in the memory to individual rows.

Sixteen words are provided in the display memory for this purpose. The lower 10 bits address the first word in the memory where the row data starts. This value is an offset in terms of 16-bit words from the start of Display memory (8000H). The most significant bit enables the display when not within the scroll (dynamic) area.

The display map memory is fixed at the first 16 words in the Closed Caption display memory.

Table 19 Display map bit allocation

| BIT | FUNCTION |
|--------|---|
| 11 | Text display enable, valid outside soft scroll area. 0 = disable; 1 = enable. |
| 10 | This bit is reserved, should be set to logic 0. |
| 9 to 0 | Pointer to row data. |

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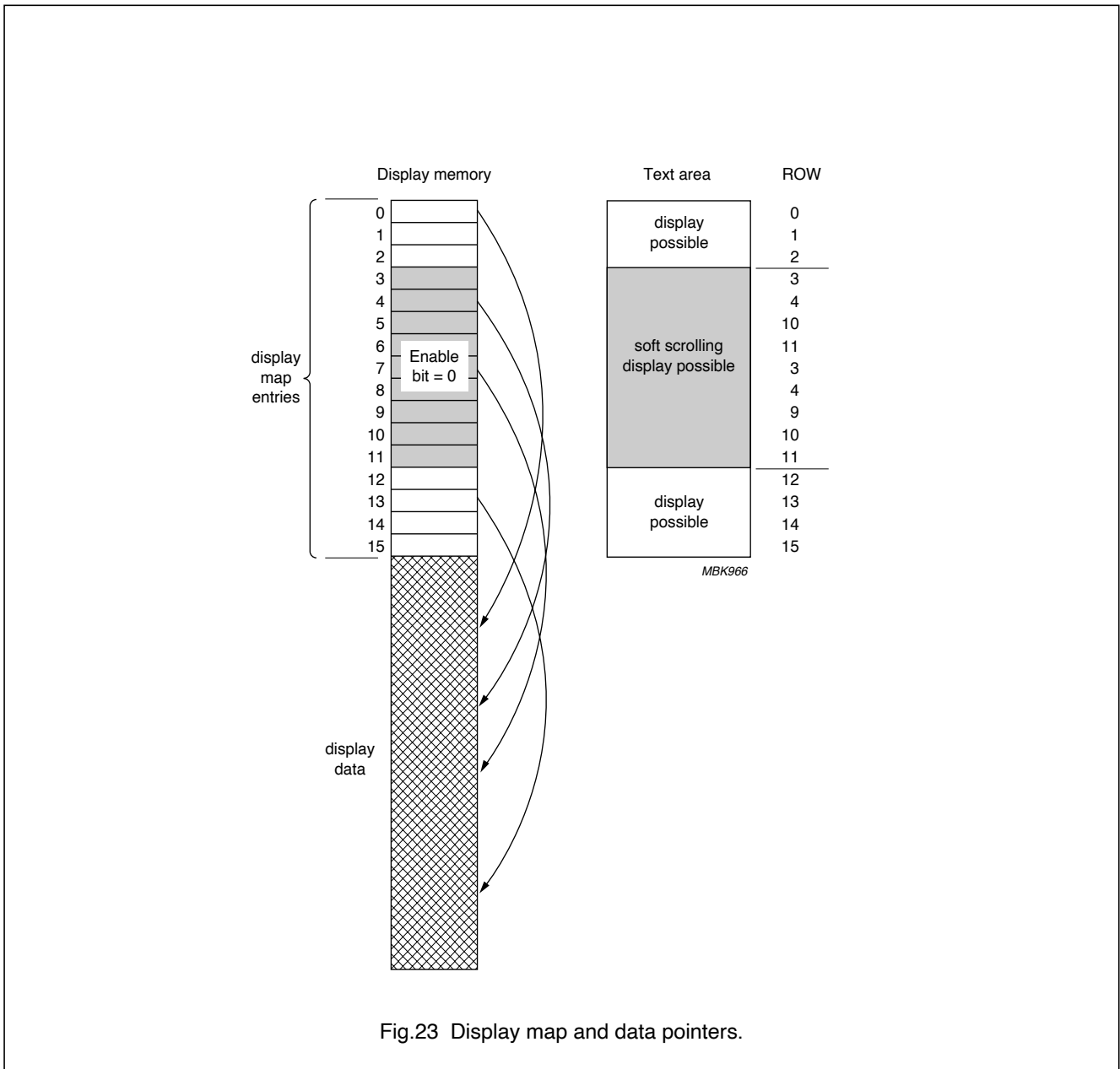


Fig.23 Display map and data pointers.

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18.6.3 SOFT SCROLL ACTION

The dynamic scroll region is defined by the MMR Scroll Area, MMR Scroll Range, MMR Top Scroll line and the MMR Status. The scroll area is enabled when the SCON bit is set in MMR Status.

The position of the soft scroll area window is defined using the Soft Scroll Position (SSP<3:0>), and the height of the window is defined using the Soft Scroll Height (SSH<3:0>) both are in MMR Scroll Range. The rows that are scrolled through the window are defined using the Start Scroll Row (STS<3:0>) and the Stop Scroll Row (SPS<3:0>) both are in MMR Scroll Area.

The soft scrolling function is done by modifying the Scroll Line (SCL<3:0>) in MMR Top Scroll Line. and the first scroll row value SCR<3:0> in the MMR Status.

If the number of rows allocated to the scroll counter is larger than the defined visible scroll area, this allows parts of rows at the top and bottom to be displayed during the scroll function. The registers can be written throughout the field and the values are updated for display with the next field sync. Care should be taken that the register pairs are written to by the software in the same field.

Only a region that contains only single height rows or only double height rows can be scrolled.

TXT: The display is organised as a fixed size of 25 rows (0 to 24) of 40 columns (0 to 39), This is the standard size for teletext transmissions. The control data in row 25 is not displayed but is used to configure the display page correctly.

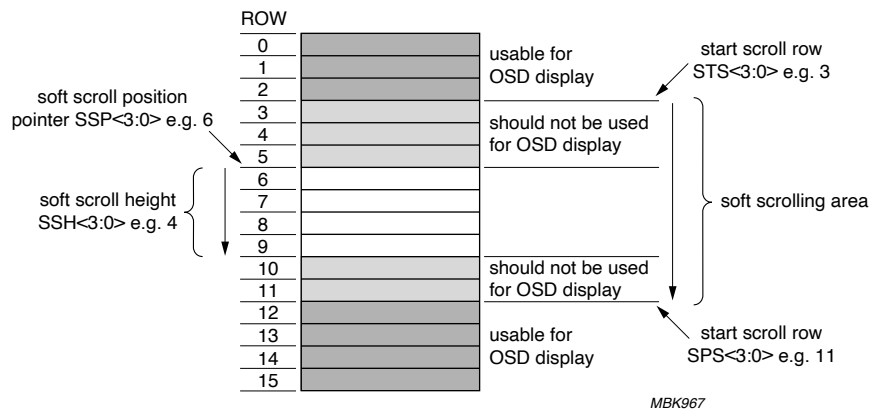


Fig.24 Soft scroll area.

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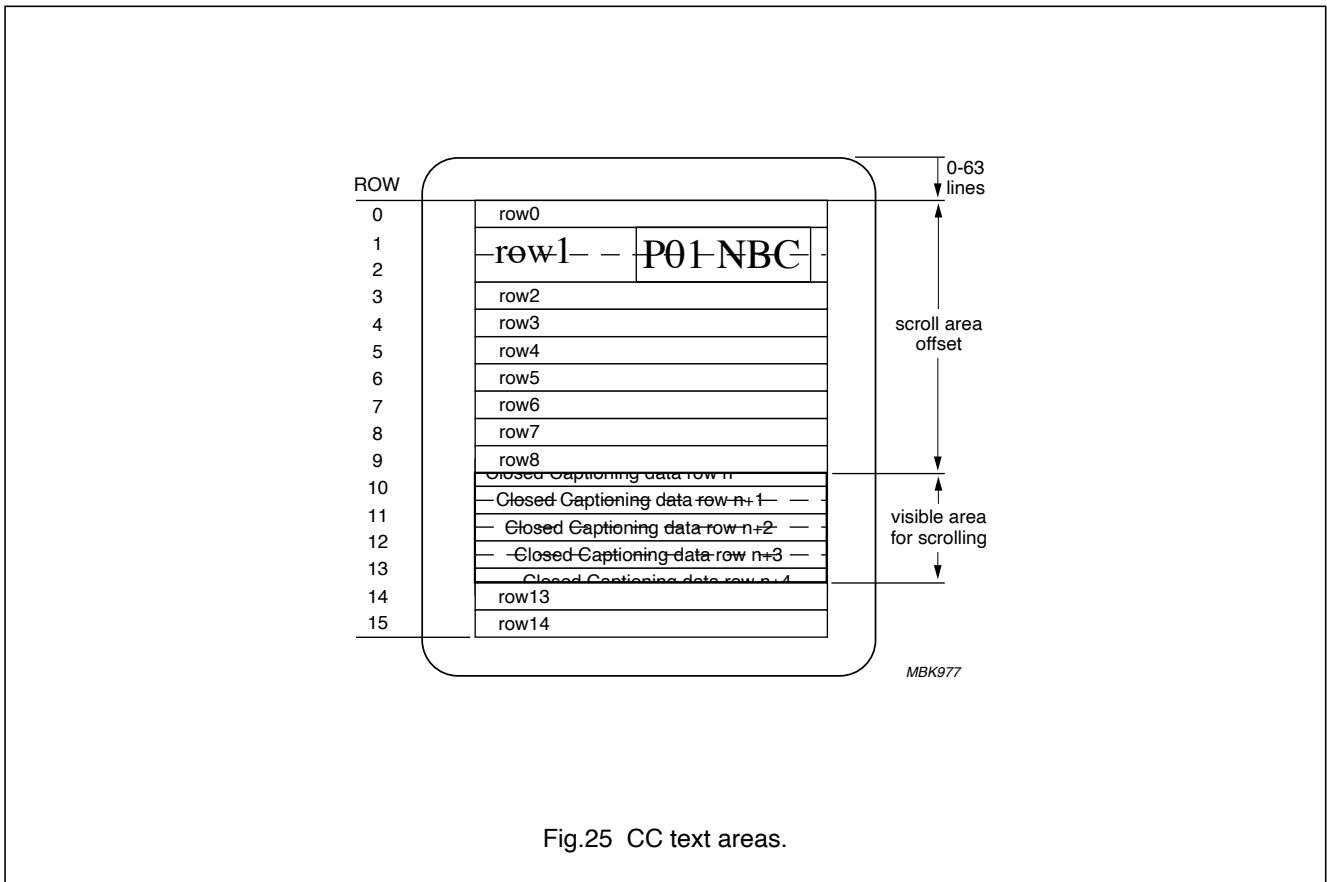
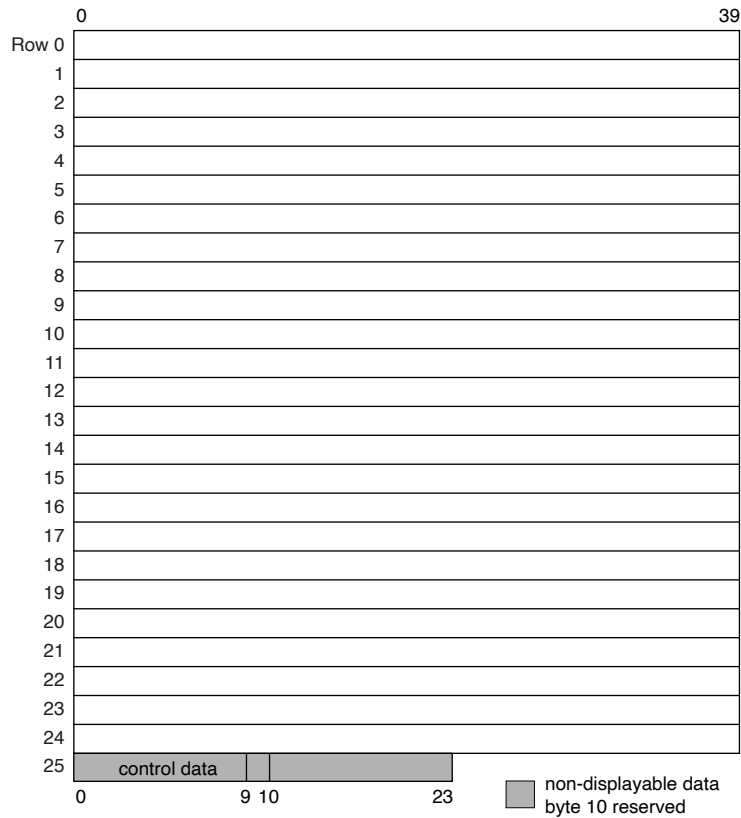


Fig.25 CC text areas.

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Fig.26 TXT text area.

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18.7 Display positioning

The display consists of the **screen colour** covering the whole screen and the **text area** that is placed within the visible screen area.

The screen colour extends over a large vertical and horizontal range so that no offset is needed. The text area is offset in both directions relative to the vertical and horizontal sync pulses.

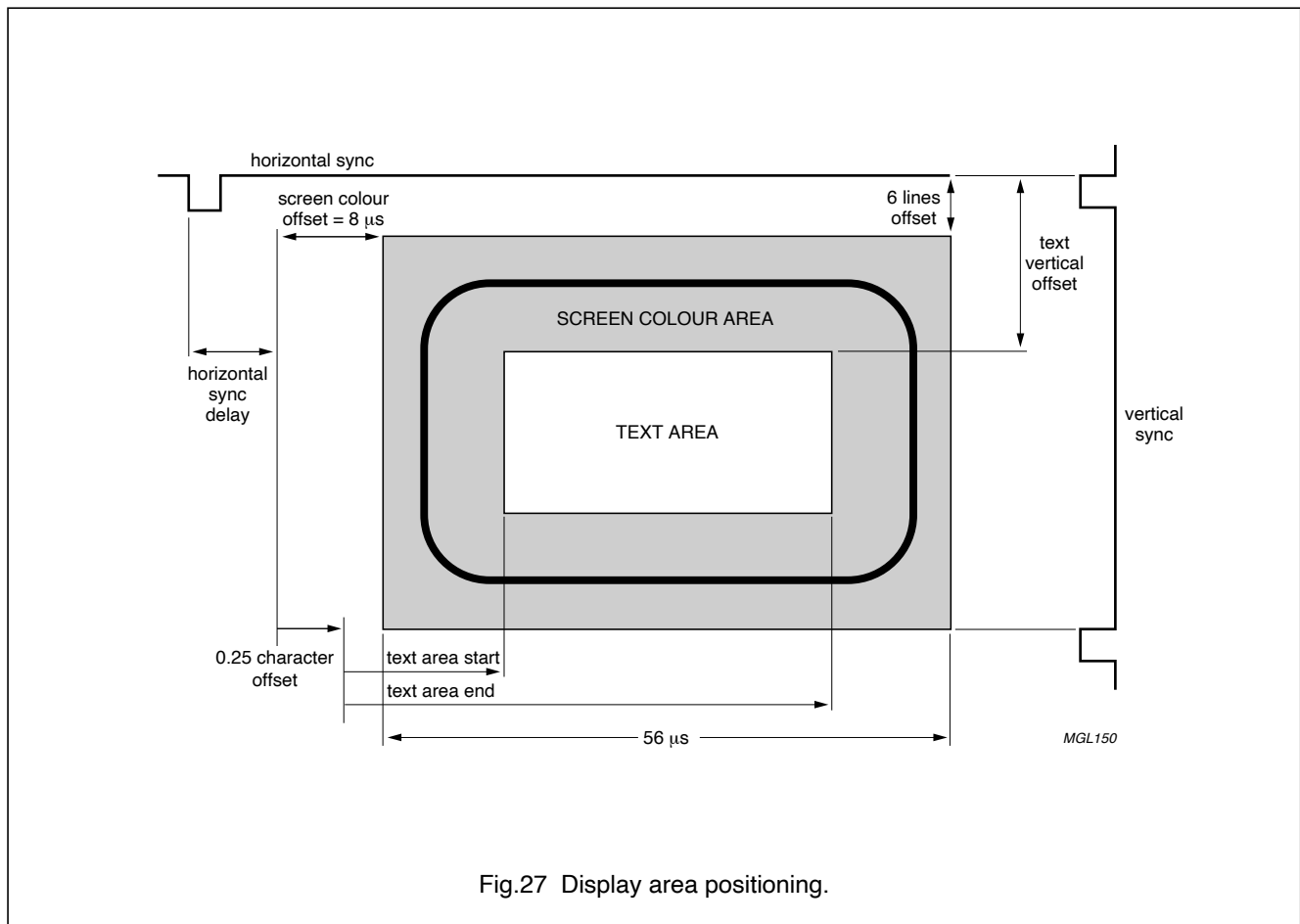


Fig.27 Display area positioning.

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18.7.1 SCREEN COLOUR DISPLAY AREA

This area is covered by the screen colour. The screen colour display area starts with a fixed offset of 8 μ s from the leading edge of the horizontal sync pulse in the horizontal direction. A vertical offset is not necessary.

Table 20 Screen colour display area

| POSITION | 525-LINE |
|------------|--|
| Horizontal | Start at 8 μ s after leading edge of horizontal sync for 56 μ s. |
| Vertical | Line 9, Field 1 (321, Field 2) to leading edge of vertical sync (line numbering using 625 standard). |

18.7.2 TEXT DISPLAY AREA

The text area can be defined to start with an offset in both the horizontal and vertical direction.

Table 21 Text display area

| POSITION | DESCRIPTION |
|------------|---|
| Horizontal | Up to 48 full sized characters per row. Start position setting from 8 to 64 characters from the leading edge of horizontal sync. Fine adjustment in quarter characters. |
| Vertical | 256 lines (nominal 41 to 297). Start position setting from leading edge of vertical sync, legal values are 4 to 64 lines (line numbering using 625 standard). |

The horizontal offset is set in the MMR Text Area Start. The offset is done in full width characters using TAS<5:0> and quarter characters using HOP<1:0> for fine setting. The values 00H to 08H for TAS<5:0> will result in a corrupted display.

The width of the text area is defined in the MMR Text Area End Register by setting the end character value TAE<5:0>. This number determines where the background colour of the Text Area will end if set to extend to the end of the row. It will also terminate the character fetch process thus eliminating the necessity of a **row end** attribute. This entails however writing to all positions.

The vertical offset is set in the MMR Text Position Vertical. The offset value VOL<5:0> is done in number of TV scan lines.

Note that the Text Position Vertical Register should not be set to 00H as the Display Busy interrupt is not generated in these circumstances.

18.8 Character set

To facilitate the global nature of the device the character set has the ability to accommodate a large number of characters, which can be stored in different matrices.

18.8.1 CHARACTER MATRICES

The character matrices that can be accommodated in both display modes are:

(H \times V \times planes) 12 \times 9 \times 1, 12 \times 10 \times 1, 12 \times 13 \times 1, 12 \times 16 \times 1.

These modes allow two colours per character position.

In CC mode two additional character matrices are available to allow four colours per character.

(H \times V \times planes) 12 \times 13 \times 2, 12 \times 16 \times 2.

The characters are stored physically in ROM in a matrix of size either 12 \times 10 or 12 \times 16.

18.8.2 CHARACTER SET SELECTION

Four character sets are available in the device. A set can consist of alphanumeric characters as required by the WST or US Closed Captioning, Customer definable On-Screen Display characters, and Special Graphic characters.

CC: Only a single character set can be used for display and this is selected using the Basic Set selection TXT18.BS<1:0>. When selecting a character set in CC mode, the Twist Set selection TXT19.TS<1:0> should be set to the same value as TXT18.BS<1:0> for correct operation.

TXT: Two character sets can be displayed at once. These are the basic G0 set or the alternative G0 set (Twist Set). The basic set is selected using TXT18.BS<1:0>. The alternative/twist character set is defined by TXT19.TS<1:0>. Since the alternative character set is an option it can be enabled or disabled using TXT19.TEN, and the language code that is defined for the alternative set is defined by TXT19.TC<2:0>.

The National option table is selected using TXT18.NOT<3:0>. A maximum of 31 National option tables can be defined when combined with the EAST/WEST control bit located in register TXT4.

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An example of the character set selection and definitions is shown in Table 22.

An example of the National option reference table is shown in Table 23. Only a certain number of national options will be relevant for each of the Character sets.

Table 22 Character set selection

| BS1/TS1 | BS0/TS0 | CHARACTER SET | EXAMPLE LANGUAGE |
|---------|---------|---------------|------------------|
| 0 | 0 | Set 0 | Latin |
| 0 | 1 | Set 1 | Greek |
| 1 | 0 | Set 2 | - |
| 1 | 1 | Set 3 | Closed Caption |

Table 23 National option selection

| C12 | C13 | C14 | NOT<3:0> = 0000 | NOT<3:0> = 0001 | NOT<3:0> = 0010 | ... | NOT<3:0> = 1110 |
|-----|-----|-----|-----------------|-----------------|-----------------|-----|-----------------|
| 0 | 0 | 0 | English | Polish | English | ... | Polish |
| 0 | 0 | 1 | German | German | German | ... | German |
| 0 | 1 | 0 | Swedish | Swedish | Swedish | ... | Estonian |
| 0 | 1 | 1 | Italian | Italian | Italian | ... | Lettish |
| 1 | 0 | 0 | French | French | French | ... | Russian |
| 1 | 0 | 1 | Spanish | - | Spanish | ... | Serb-Croat |
| 1 | 1 | 0 | Czech | Czech | Turkish | ... | Czech |
| 1 | 1 | 1 | - | - | - | ... | - |

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18.9 ROM addressing

Three ROMs are used to generate the correct pixel information. The first contains the National option look-up table, the second contains the Basic character look-up table and the third contains the Character pixel information.

Although these are individual ROMs, since they do not need to be accessed simultaneously they are all combined into a single ROM unit.

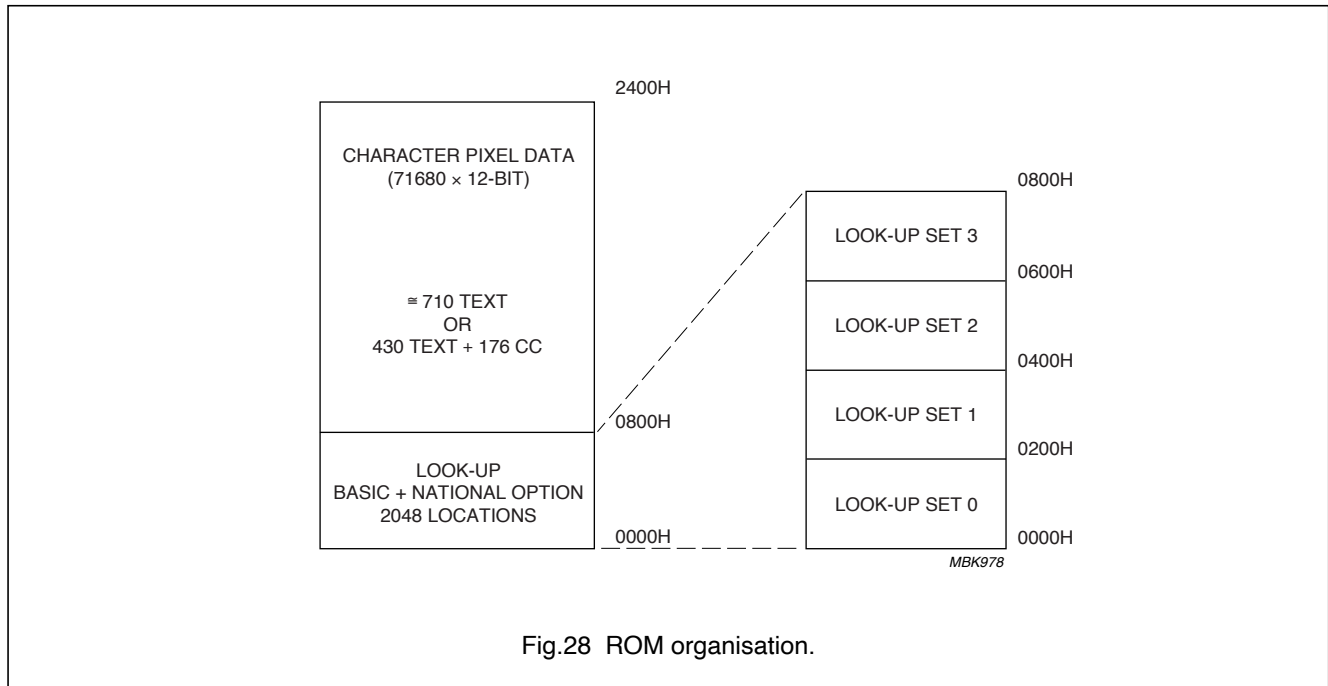


Fig.28 ROM organisation.

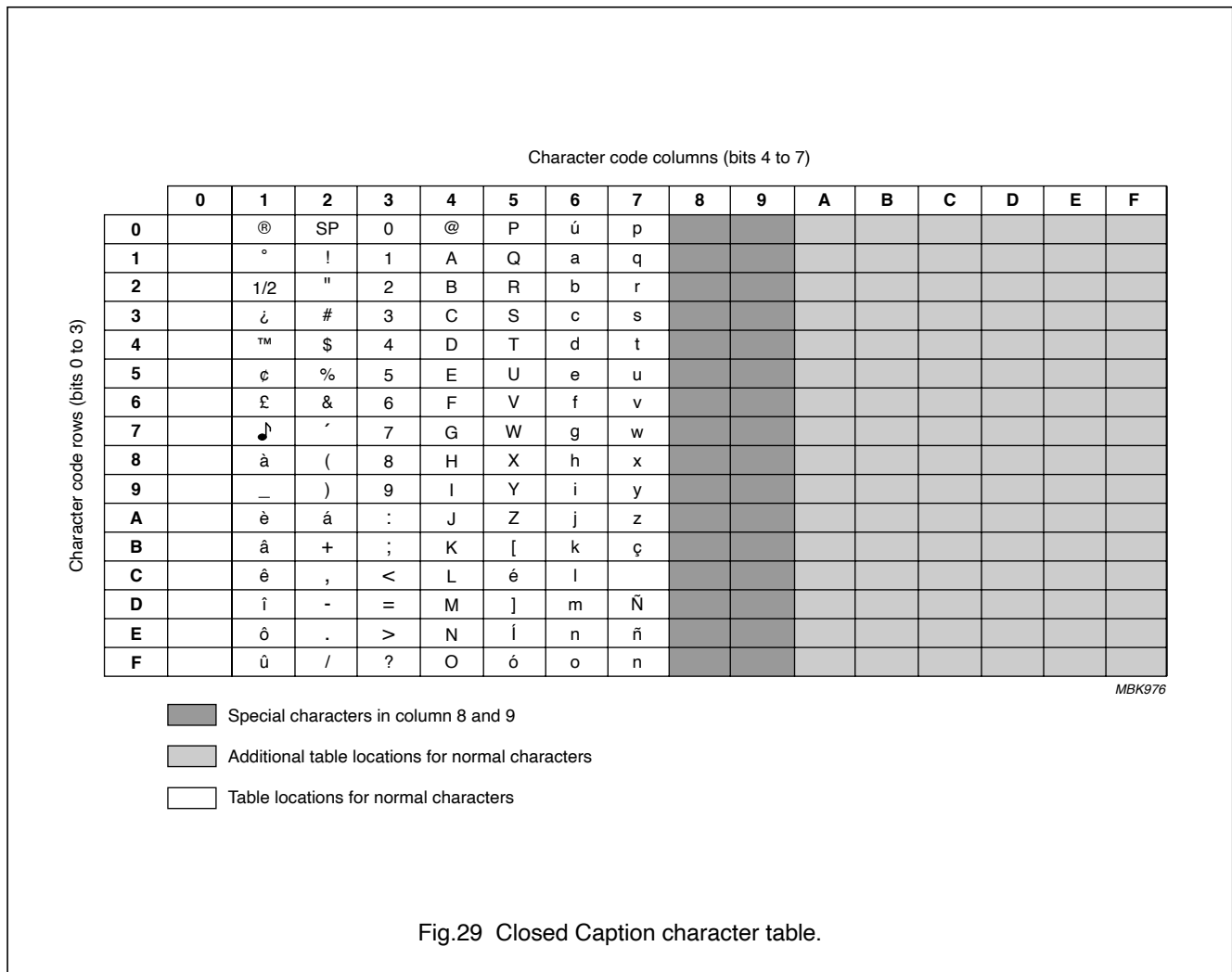
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18.9.1 CHARACTER TABLE

CC: The character table is shown in Fig.29.

TXT: One of the character set options (Pan-European: Latin) is shown in Fig.22.



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18.10 Redefinable characters

A number of Dynamically Redefinable Characters (DRCs) are available. These are mapped onto the normal character codes, and replace the predefined ROM value.

There are 32 DRCs, the first 16 occupy the character codes 80H to 8FH, the second 16 occupy the locations 90H to 9FH. This allows for 32 DRCs or 16 Special DRCs.

The remapping of the standard OSD to the DRCs is activated when the TXT20.DRCS ENABLE bit is set. The selection of Normal or Special OSD symbols is defined by the TXT20.OSD PLANES.

Each character is stored in a matrix of $12 \times 16 \times 1$ (V x H x planes), this allows for all possible character matrices to be defined within a single location.

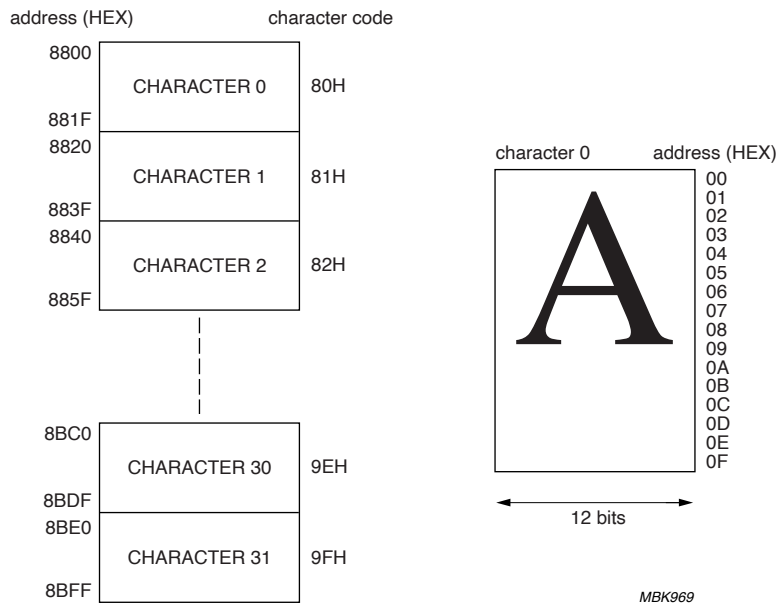


Fig.30 Organisation of DRC RAM.

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18.11 Display synchronization

The horizontal and vertical synchronizing signals from the TV deflection are used as inputs. Both signals can be inverted before being delivered to the Phase Selector section.

CC: The polarity is controlled using either VPOL or HPOL bits in the MMR Text Position Vertical.

TXT: The TXT1.H POLARITY and TXT1.V POLARITY bits control the polarity.

A line locked 12 MHz clock is derived from the 12 MHz free running oscillator by the Phase Selector. This line locked clock is used to clock the whole of the Display block.

The horizontal and vertical sync signals are synchronized with the 12 MHz clock before being used in the display section.

18.12 Video/Data switch (Fast Blanking) polarity

The polarity of the video/data (Fast Blanking) signal can be inverted. The polarity is set with the VDSPOL bit in the MMR RGB Brightness.

Table 24 Fast blanking signal polarity

| VDSPOL | VDS | CONDITION |
|--------|-----|---------------|
| 0 | 1 | RGB display |
| 0 | 0 | Video display |
| 1 | 0 | RGB display |
| 1 | 1 | Video display |

18.13 Video/data switch adjustment

To take into account the delay between the RGB values and the VDS signal due to external buffering, the VDS signal can be moved in relation to the RGB signals. The VDS signal can be set to be either a clock cycle before or after the RGB signal, or coincident with the RGB signal. This is done using VDEL<2:0> in the MMR Configuration.

18.14 RGB brightness control

A brightness control is provided to allow the RGB upper output voltage level to be modified. The nominal value is 1 V into a 150 Ω resistor, but can be varied between 0.7 V and 1.2 V.

The brightness is set in MMR RGB Brightness.

Table 25 RGB brightness

| BRI3 TO BRI0 | RGB BRIGHTNESS |
|--------------|----------------|
| 0000 | lowest value |
| ... | ... |
| 1111 | highest value |

18.15 Contrast reduction

CC: This feature is not available in CC mode.

TXT: The $\overline{\text{COR}}$ bits in SFRs TXT5 and TXT6 control when the $\overline{\text{COR}}$ output of the device is activated (i.e. pulled LOW). This output is intended to act on the TV's display circuits to reduce contrast of the video when it is active. The result of contrast reduction is to improve the readability of the text in a mixed teletext and video display.

The bits in the TXT5 and TXT6 SFRs allow the display to be set up so that, for example, the areas inside teletext boxes will be contrast reduced when a subtitle is being displayed but that the rest of the screen will be displayed as normal video.

19 MEMORY MAPPED REGISTERS (MMR)

The memory mapped registers are used to control the display. The registers are mapped into the microcontroller MOVX address space, starting at address 87F0H and extending to 87FFH.

Table 26 MMR address summary

| REGISTER NUMBER | MEMORY ADDRESS | FUNCTION |
|-----------------|----------------|------------------------|
| 0 | 87F0H | Display Control |
| 1 | 87F1H | Text Position Vertical |
| 2 | 87F2H | Text Area Start |
| 3 | 87F3H | Fringing Control |
| 4 | 87F4H | Text Area End |
| 5 | 87F5H | Scroll Area |
| 6 | 87F6H | Scroll Range |
| 7 | 87F7H | RGB Brightness |
| 8 | 87F8H | Status |
| 9 | 87F9H | reserved |
| 10 | 87FAH | reserved |
| 11 | 87FBH | reserved |
| 12 | 87FCH | HSYNC Delay |
| 13 | 87FDH | VSYNC Sync Delay |
| 14 | 87FEH | Top Scroll Line |
| 15 | 87FFH | Configuration |

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Table 27 MMR map

| ADD | R/W | NAME | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | RESET |
|------|-----|------------------------|--------|-------|-------|-------|-------|------|------|------|-------|
| 87F0 | R/W | Display Control | SRC3 | SRC2 | SRC1 | SRC0 | - | MSH | MOD1 | MOD0 | 00H |
| 87F1 | R/W | Text Position Vertical | VPOL | HPOL | VOL5 | VOL4 | VOL3 | VOL2 | VOL1 | VOL0 | 00H |
| 87F2 | R/W | Text Area Start | HOP1 | HOP0 | TAS5 | TAS4 | TAS3 | TAS2 | TAS1 | TAS0 | 00H |
| 87F3 | R/W | Fringing Control | FRC3 | FRC2 | FRC1 | FRC0 | FRDN | FRDE | FRDS | FRDW | 00H |
| 87F4 | R/W | Text Area End | - | - | TAE5 | TAE4 | TAE3 | TAE2 | TAE1 | TAE0 | 00H |
| 87F5 | R/W | Scroll Area | SSH3 | SSH2 | SSH1 | SSH0 | SSP3 | SSP2 | SSP1 | SSP0 | 00H |
| 87F6 | R/W | Scroll Range | SPS3 | SPS2 | SPS1 | SPS0 | STS3 | STS2 | STS1 | STS0 | 00H |
| 87F7 | R/W | RGB Brightness | VDSPOL | - | - | - | BRI3 | BRI2 | BRI1 | BRI0 | 00H |
| 87F8 | R | Status | BUSY | FIELD | SCON | FLR | SCR3 | SCR2 | SCR1 | SCR0 | 00H |
| | W | | - | - | SCON | FLR | SCR3 | SCR2 | SCR1 | SCR0 | 00H |
| 87FC | R/W | HSYNC Delay | - | HSD6 | HSD5 | HSD4 | HSD3 | HSD3 | HSD1 | HSD0 | 00H |
| 87FD | R/W | VSYNC Delay | - | VSD6 | VSD5 | VSD4 | VSD3 | VSD2 | VSD1 | VSD0 | 00H |
| 87FE | R/W | Top Scroll Line | - | - | - | - | SCL3 | SCL2 | SCL1 | SCL0 | 00H |
| 87FF | R/W | Configuration | CC | VDEL2 | VDEL1 | VDEL0 | TXT/V | - | - | - | 00H |

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Table 28 MMR bit definition

| REGISTER BIT | FUNCTION |
|-------------------------------|--|
| Display Control | |
| SRC3 to SRC0 | screen colour definition |
| MSH | meshing all background colours (logic 1) |
| MOD1 to MOD0 | 00 = Video 01 = Full Text 10 = Mixed Screen Colour 11 = Mixed Video |
| Text Position Vertical | |
| VPOL | inverted input polarity (logic 1) |
| HPOL | inverted input polarity (logic 1) |
| VOL5 to VOL0 | display start vertical offset from VSYNC (lines) |
| Text Area Start | |
| HOP1 to HOP0 | fine horizontal offset in quarter of characters |
| TAS5 to TAS0 | text area start |
| Fringing Control | |
| FRC3 to FRC0 | fringing colour, value address of CLUT |
| FRDN | fringe in north direction (logic 1) |
| FRDE | fringe in east direction (logic 1) |
| FRDS | fringe in south direction (logic 1) |
| FRDW | fringe in west direction (logic 1) |
| Text Area End | |
| TAE5 to TAE0 | text area end, in full characters |
| Scroll Area | |
| SSH3 to SSH0 | soft scroll height |
| SSP3 to SSP0 | soft scroll position |
| Scroll Range | |
| SPS3 to SPS0 | stop scroll row |
| STS3 to STS0 | start scroll row |
| RGB Brightness | |
| VDSPOL | VDS polarity 0 = RGB (1), Video (0) 1 = RGB (0), Video (1) |
| BRI3 to BRI0 | RGB brightness control |

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| REGISTER BIT | FUNCTION |
|------------------------|--|
| Status read | |
| BUSY | access to display memory could cause display problems (logic 1) |
| FIELD | even field (logic 1) |
| FLR | active flash region background only displayed (logic 1) |
| SCR3 to SCR0 | first scroll row |
| Status write | |
| SCON | scroll area enabled (logic 1) |
| FLR | active flash region background colour only displayed (logic 1) |
| SCR3 to SCR0 | first scroll row |
| HSYNC Delay | |
| HSD6 to HSD0 | HSYNC delay, in full size characters |
| VSYNC Delay | |
| VSD6 to VSD0 | VSYNC delay in number of 8-bit 12 MHz clock cycles |
| Top Scroll Line | |
| SCL3 to SCL0 | top line for scroll |
| Configuration | |
| CC | closed caption mode (logic 1) |
| VDEL2 to VDEL0 | pixel delay between VDS and RGB output 000 = VDS switched to video, not active 001 = VDS active one pixel earlier then RGB 010 = VDS synchronous to RGB 100 = VDS active one pixel after RGB |
| TXT/V | BUSY signal switch; horizontal (logic 1) |

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20 LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|------------------|----------------------------------|------------|------|------------------------------|------|
| V _{DDX} | supply voltage (all supplies) | | -0.5 | +4.0 | V |
| V _I | input voltage (any input) | note 1 | -0.5 | V _{DD} + 0.5 or 4.1 | V |
| V _O | output voltage (any output) | note 1 | -0.5 | V _{DD} + 0.5 | V |
| I _O | output current (each output) | | - | ±10 | mA |
| I _{IOK} | DC input or output diode current | | - | ±20 | mA |
| T _{amb} | operating ambient temperature | | -20 | +70 | °C |
| T _{stg} | storage temperature | | -55 | +125 | °C |

Note

1. This maximum value refers to 5 V tolerant I/Os and may be 6 V maximum, but only when V_{DD} is present.

21 CHARACTERISTICS

V_{DD} = 3.3 V ± 10%; V_{SS} = 0 V; T_{amb} = -20 to +70 °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------------|--|----------------------------------|-------|-------|-------|------|
| Supplies | | | | | | |
| V _{DDX} | any supply voltage (V _{DD} to V _{SS}) | | 3.0 | 3.3 | 3.6 | V |
| I _{DDP} | Periphery supply current | note 1 | 1 | - | - | mA |
| I _{DDC} | core supply current | | - | 12 | 18 | mA |
| I _{DDC(id)} | Idle mode core supply current | | - | 383 | 600 | µA |
| I _{DDC(pd)} | Power-down mode core supply current | | - | 666 | 900 | µA |
| I _{DDC(stb)} | Standby mode core supply current | | - | 5.1 | 9 | mA |
| I _{DDA} | analog supply current | | - | 45 | 48 | mA |
| I _{DDA(id)} | Idle mode analog supply current | | - | 444 | 700 | µA |
| I _{DDA(pd)} | Power-down mode analog supply current | | - | 433 | 700 | µA |
| I _{DDA(stb)} | Standby mode analog supply current | | - | 809 | 950 | µA |
| Digital inputs | | | | | | |
| RESET | | | | | | |
| V _{IL} | LOW-level input voltage | | - | - | 1.34 | V |
| V _{IH} | HIGH-level input voltage | | 1.49 | - | 5.5 | V |
| V _{hys} | hysteresis voltage of Schmitt trigger input | | 0.44 | - | 0.58 | V |
| I _{LI} | input leakage current | V _I = 0 | - | - | 0.17 | µA |
| R _{pd} | equivalent pull-down resistance | V _I = V _{DD} | 55.73 | 70.71 | 92.45 | kΩ |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|---|--|------|------|-------|------|
| HSYNC AND VSYNC | | | | | | |
| V _{IL} | LOW-level input voltage | | – | – | 1.31 | V |
| V _{IH} | HIGH-level input voltage | | 1.44 | – | 5.5 | V |
| V _{hys} | hysteresis voltage of Schmitt trigger input | | 0.40 | – | 0.56 | V |
| I _{LI} | input leakage current | V _I = 0 to V _{DD} | – | – | 0.00 | μA |
| Digital outputs | | | | | | |
| FRAME, VDS | | | | | | |
| V _{OL} | LOW-level output voltage | I _{OL} = 3 mA | – | – | 0.13 | V |
| V _{OH} | HIGH-level output voltage | I _{OH} = 3 mA | 2.84 | – | – | V |
| t _r | output rise time | 10% to 90%; C _L = 70 pF | 7.50 | 8.85 | 10.90 | ns |
| t _f | output fall time | 10% to 90%; C _L = 70 pF | 6.70 | 7.97 | 10.00 | ns |
| COR (OPEN-DRAIN OUTPUT) | | | | | | |
| V _{OL} | LOW-level output voltage | I _{OL} = 3 mA | – | – | 0.14 | V |
| V _{OH} | HIGH-level pull-up output voltage | I _{OL} = –3 mA; push-pull | 2.84 | – | – | V |
| V _{IL} | LOW-level input voltage | | – | – | 0.00 | V |
| V _{IH} | HIGH-level input voltage | | 0.00 | – | 5.50 | V |
| I _{LI} | input leakage current | V _I = 0 to V _{DD} | – | – | 0.12 | μA |
| t _r | output rise time | 10% to 90%; C _L = 70 pF | 7.20 | 8.64 | 11.10 | ns |
| | output fall time | 10% to 90%; C _L = 70 pF | 4.90 | 7.34 | 9.40 | ns |
| Digital input/outputs | | | | | | |
| P0.0 TO P0.4, P0.7, P1.0 TO P1.1, P2.1 TO P2.7, P3.0 TO P3.7 | | | | | | |
| V _{IL} | LOW-level input voltage | | – | – | 1.28 | V |
| V _{IH} | HIGH-level input voltage | | 1.43 | – | 5.50 | V |
| V _{hys} | hysteresis voltage of Schmitt trigger input | | 0.41 | – | 0.55 | V |
| I _{LI} | input leakage current | V _I = 0 to V _{DD} | – | – | 0.01 | μA |
| V _{OL} | LOW-level output voltage | I _{OL} = 4 mA | – | – | 0.18 | V |
| V _{OH} | HIGH-level output voltage | I _{OH} = –4 mA push-pull | 2.81 | – | 5.50 | V |
| t _r | output rise time | 10% to 90%; C _L = 70 pF push-pull | 6.50 | 8.47 | 10.70 | ns |
| t _f | output fall time | 10% to 90%; C _L = 70 pF | 5.70 | 7.56 | 10.00 | ns |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------------------------------|--|--|-------|-------|--------|------|
| P1.2, P1.3 AND P2.0 | | | | | | |
| V _{IL} | LOW-level input voltage | | – | – | 1.29 | V |
| V _{IH} | HIGH-level input voltage | | 1.45 | – | 5.50 | V |
| V _{hys} | hysteresis voltage of Schmitt trigger input | | 0.42 | – | 0.56 | V |
| I _{LI} | input leakage current | V _I = 0 to V _{DD} | – | – | 0.02 | μA |
| V _{OL} | LOW-level output voltage | I _{OL} = 4 mA | – | – | 0.17 | V |
| V _{OH} | HIGH-level output voltage | I _{OH} = –4 mA push-pull | 2.81 | – | 5.50 | V |
| t _r | output rise time | 10% to 90%; C _L = 70 pF push-pull | 7.00 | 8.47 | 10.50 | ns |
| t _f | output fall time | 10% to 90%; C _L = 70 pF | 5.40 | 7.36 | 9.30 | ns |
| P0.5 AND P0.6 | | | | | | |
| V _{IL} | LOW-level input voltage | | – | – | 1.28 | V |
| V _{IH} | HIGH-level input voltage | | 1.43 | – | 5.50 | V |
| I _{LI} | input leakage current | V _I = 0 to V _{DD} | – | – | 0.11 | μA |
| V _{hys} | hysteresis of Schmitt trigger input | | 0.42 | – | 0.58 | V |
| V _{OL} | LOW-level output voltage | I _{OL} = 8 mA | – | – | 0.20 | V |
| V _{OH} | HIGH-level output voltage | I _{OH} = –8 mA push-pull | 2.76 | – | 5.50 | V |
| t _r | output rise time | 10% to 90%; C _L = 70 pF push-pull | 7.40 | 8.22 | 8.80 | ns |
| t _f | output fall time | 10% to 90%; C _L = 70 pF | 4.20 | 4.57 | 5.20 | ns |
| P1.4 TO P1.7 (OPEN-DRAIN) | | | | | | |
| V _{IL} | LOW-level input voltage | | – | – | 1.45 | V |
| V _{IH} | HIGH-level input voltage | | 1.62 | – | 5.5 | V |
| V _{hys} | hysteresis voltage of Schmitt trigger input | | 0.49 | – | 0.60 | V |
| I _{LI} | input leakage current | V _I = 0 to V _{DD} | – | – | 0.13 | μA |
| V _{OL} | LOW-level output voltage | I _{OL} = 8 mA | – | – | 0.35 | V |
| t _f | output fall time | 10% to 90%; C _L = 70 pF | 69.70 | 83.67 | 103.30 | ns |
| Analog inputs | | | | | | |
| CVBS0 AND CVBS1 | | | | | | |
| V _{sync} | sync voltage amplitude | | 0.1 | 0.3 | 0.6 | V |
| V _{vid(p-p)} | video input voltage amplitude (peak-to-peak value) | | 0.7 | 1.0 | 1.4 | V |
| Z _{source} | source impedance | | 0 | – | 250 | Ω |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------------------------|--|--|-----------|------|-----------------|------------|
| V_{IH} | HIGH-level input voltage | | 3.0 | – | $V_{DDA} + 0.3$ | V |
| C_I | input capacitance | | – | – | 10 | pF |
| IREF | | | | | | |
| R_{gnd} | resistor to ground | resistor tolerance 2% | – | 24 | – | k Ω |
| ADC0 TO ADC3 | | | | | | |
| V_{IH} | HIGH-level input voltage | | – | – | V_{DDA} | V |
| C_I | input capacitance | | – | – | 10 | pF |
| VPE | | | | | | |
| V_{IH} | HIGH-level input voltage | | – | – | 9.0 | V |
| Analog outputs | | | | | | |
| R, G AND B | | | | | | |
| I_{OL} | output current (Black Level) | $V_{DDA} = 3.3$ V | –10 | – | +10 | μ A |
| I_{OH} | output current (maximum Intensity) | $V_{DDA} = 3.3$ V Intensity level code = 15 dec | 6.0 | 6.67 | 7.3 | mA |
| | output current (70% of full Intensity) | $V_{DDA} = 3.3$ V Intensity level code = 0 dec | 4.2 | 4.7 | 5.1 | mA |
| R_{load} | load resistor to V_{SSA} | resistor tolerance 5% | – | 150 | – | Ω |
| C_L | load capacitance | | – | – | 15 | pF |
| Analog input/output | | | | | | |
| SYNC_FILTER | | | | | | |
| C_{sync} | storage capacitor to ground | | – | 100 | – | nF |
| V_{sync} | sync filter level voltage for nominal sync amplitude | | 0.35 | 0.55 | 0.75 | V |
| Crystal oscillator | | | | | | |
| XTALIN | | | | | | |
| V_{IL} | LOW-level input voltage | | V_{SSA} | – | – | V |
| V_{IH} | HIGH-level input voltage | | – | – | V_{DDA} | V |
| C_I | input capacitance | | – | – | 10 | pF |
| XTALOUT | | | | | | |
| C_O | output capacitance | | – | – | 10 | pF |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|-------------------------------|---|------|--------|--------------------------|------------------|
| Crystal specification; notes 2 and 3 | | | | | | |
| f_{xtal} | nominal frequency | fundamental mode | – | 12 | – | MHz |
| C_L | crystal load capacitance | | – | – | 30 | pF |
| C_1 | crystal motional capacitance | $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ | – | – | 20 | fF |
| R_r | resonance resistance | $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ | – | – | 60 | Ω |
| C_{osc} | capacitors at XTALIN, XTALOUT | $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ | – | note 4 | – | pF |
| C_0 | crystal holder capacitance | $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ | – | – | note 5 | pF |
| T_{xtal} | temperature range | | –20 | +25 | +85 | $^\circ\text{C}$ |
| X_j | adjustment tolerance | $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ | – | – | $\pm 50 \times 10^{-6}$ | |
| X_d | drift | | – | – | $\pm 100 \times 10^{-6}$ | |

Notes

- Peripheral current is dependent on external components and voltage levels on I/Os.
- Crystal order number 4322 143 05561.
- If the 4322 143 05561 crystal is not used, then the formulae in the crystal specification should be used. Where $C_{\text{IO}} = 7\text{ pF}$, the mean of the capacitances due to the chip at XTALIN and at XTALOUT. C_{ext} is a value for the mean of the stray capacitances due to the external circuit at XTALIN and XTALOUT. The maximum value for the crystal holder capacitance is to ensure start-up – C_{osc} may need to be reduced from the initially selected value.
- $C_{\text{osc}(\text{typ})} = 2C_L - (C_{\text{IO}} - C_{\text{ext}})$
- $C_{0(\text{max})} = 35 - \frac{1}{2}(C_{\text{osc}} + C_{\text{IO}} + C_{\text{ext}})$

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Table 29 I²C-bus characteristics

| SYMBOL | PARAMETER | FAST-MODE I ² C-bus | | UNIT |
|---------------------|--|--------------------------------|------|------|
| | | MIN. | MAX. | |
| f _{SCL} | SCL clock frequency | 0 | 400 | kHz |
| t _{BUF} | bus free time between a STOP and START condition | 1.3 | – | μs |
| t _{HD;STA} | hold time (repeated) START condition. After this period, the first clock pulse is generated. | 0.6 | – | μs |
| t _{LOW} | LOW period of the SCL clock | 1.3 | – | μs |
| t _{HIGH} | HIGH period of the SCL clock | 0.6 | – | μs |
| t _{SU;STA} | set up time for a repeated START condition | 0.6 | – | μs |
| t _{HD;DAT} | data hold time; notes 1 and 2 | 0 | 0.9 | μs |
| t _{SU;DAT} | data set up time; note 3 | 100 | – | ns |
| t _r | rise time of both SDA and SCL signals; note 4 | 20 | 300 | ns |
| t _f | fall time of both SDA and SCL signals; note 4 | 20 | 300 | ns |
| t _{SU;STO} | set up time for STOP condition | 0.6 | – | μs |
| C _b | capacitive load for each bus line | – | 400 | pF |

Notes

1. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH(min)} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
2. The maximum f_{HD;DAT} has only to be met if the device does not stretch the LOW period t_{LOW} of the SCL signal.
3. A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement t_{SU;DAT} ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250 ns (according to the standard-mode I²C-bus specification) before the SCL line is released.
4. C_b = total capacitance of one bus line in pF.

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22 QUALITY AND RELIABILITY

This device will meet Philips Semiconductors General Quality Specification for Business group "Consumer Integrated Circuits SNW-FQ-611-Part E". The principal requirements are shown in Tables 30 to 33.

Table 30 Acceptance tests per lot

| TEST | REQUIREMENTS |
|------------|-----------------------------|
| Mechanical | cumulative target: <80 ppm |
| Electrical | cumulative target: <100 ppm |

Table 31 Processability tests (by package family)

| TEST | REQUIREMENTS |
|------------------------|------------------|
| Solderability | 0/16 on all lots |
| Mechanical | 0/15 on all lots |
| Solder heat resistance | 0/15 on all lots |

Table 32 Reliability tests (by process family)

| TEST | CONDITIONS | REQUIREMENTS |
|---------------------------------|--|--|
| Operational life | 168 hours at $T_j = 150\text{ }^\circ\text{C}$ | <1000 FPM at $T_j = 150\text{ }^\circ\text{C}$ |
| Humidity life | temperature, humidity, bias 1000 hours, $85\text{ }^\circ\text{C}$, 85% RH (or equivalent test) | <2000 FPM |
| Temperature cycling performance | $T_{\text{stg}(\text{min})}$ to $T_{\text{stg}(\text{max})}$ | <2000 FPM |

Table 33 Reliability tests (by device type)

| TEST | CONDITIONS | REQUIREMENTS |
|------------------|-------------------------------------|---|
| ESD and latch-up | ESD Human body model 100 pF, 1.5 kW | 2000 V |
| | ESD Machine model 200 pF, 0 W | 200 V |
| | latch-up | 100 mA, $1.5 \times V_{\text{DD}}$ (absolute maximum) |

Notes to Tables 30 to 33

1. ppm = fraction of defective devices, in parts per million.
2. FPM = fraction of devices failing at test condition, in Failures Per Million.
3. FITS = Failures In Time Standard.

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23 APPLICATION INFORMATION

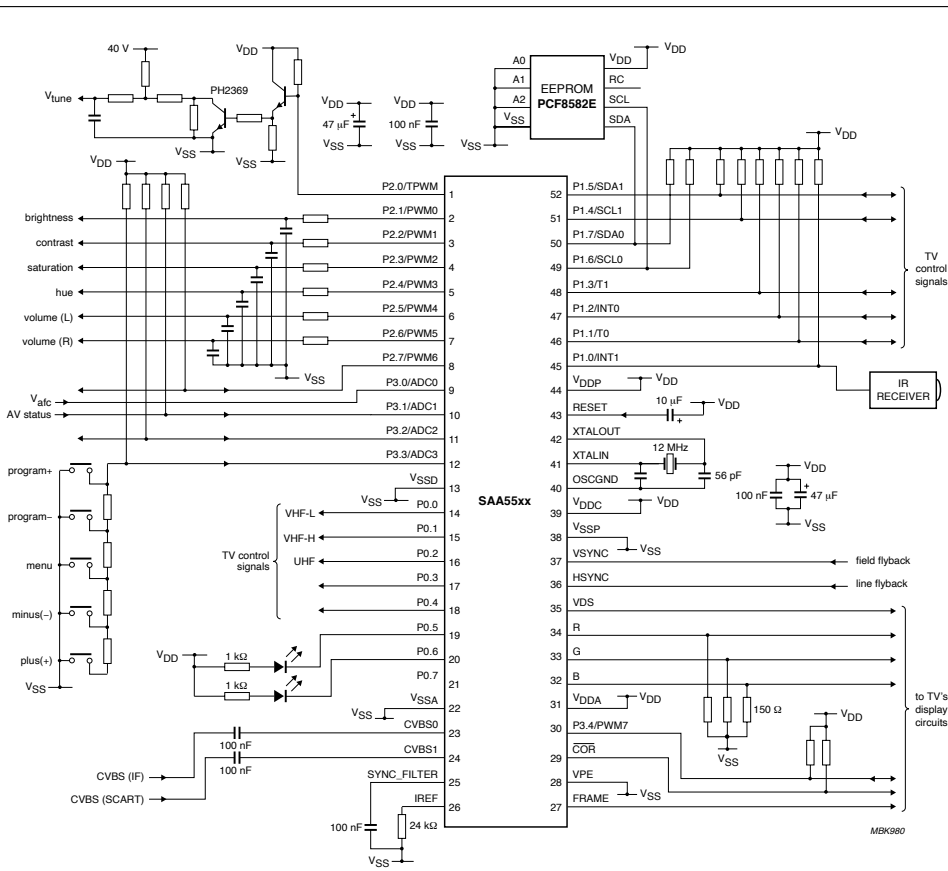


Fig.31 Application diagram.

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24 ELECTROMAGNETIC COMPATIBILITY (EMC) GUIDELINES

Optimization of circuit return paths and minimisation of common mode emission will be assisted by using a double sided printed-circuit board (PCB) with low inductance ground plane.

On a single-sided PCB a local ground plane under the whole Integrated Circuit (IC) should be present as shown in Fig.32. This should be connected by the widest possible connection back to the PCB ground connection, and bulk electrolytic decoupling capacitor. It should preferably not connect to other grounds on the way, and no wire links should be present in this connect. The use of wire links increases ground bounce by introducing inductance into the ground.

The supply pins can be decoupled at the pin to the ground plane under the IC. This is easily accomplished using surface mount capacitors, which are more effective than leaded components at high frequency.

Using a device socket will unfortunately add to the area and inductance of the external bypass loop.

A ferrite bead or inductor with resistive characteristics at high frequencies may be utilised in the supply line close to the decoupling capacitor to provide a high impedance. To prevent pollution by conduction onto the signal lines (which may then radiate) signals connected to the V_{DD} supply via a pull up resistor should not be connected to the IC side of this ferrite component.

OSCGND should be connected only to the crystal load capacitors and not the local or circuit ground.

Physical connection distances to associated active devices should be short.

Output traces should be routed with close proximity to mutually coupled ground return paths.

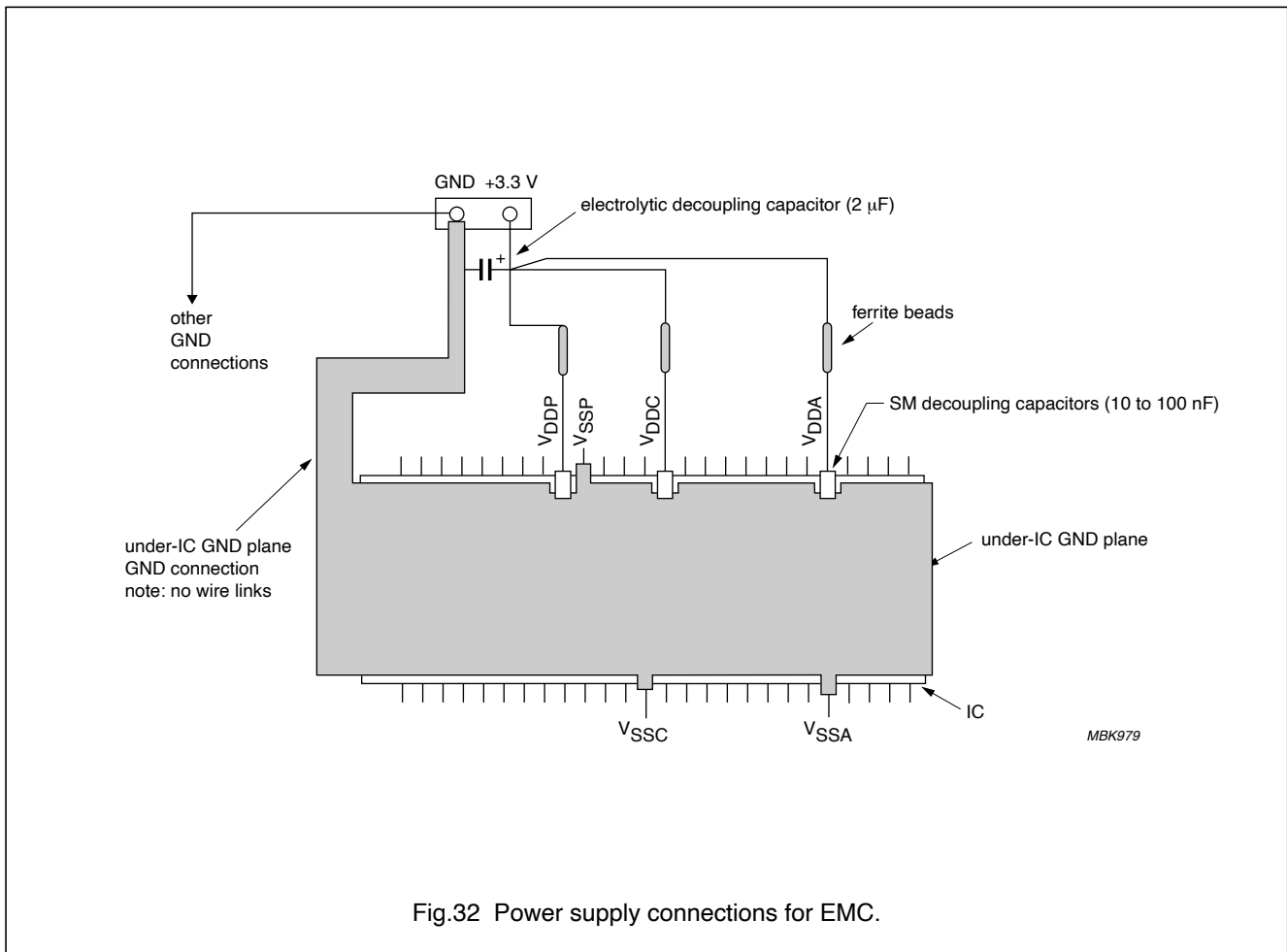


Fig.32 Power supply connections for EMC.

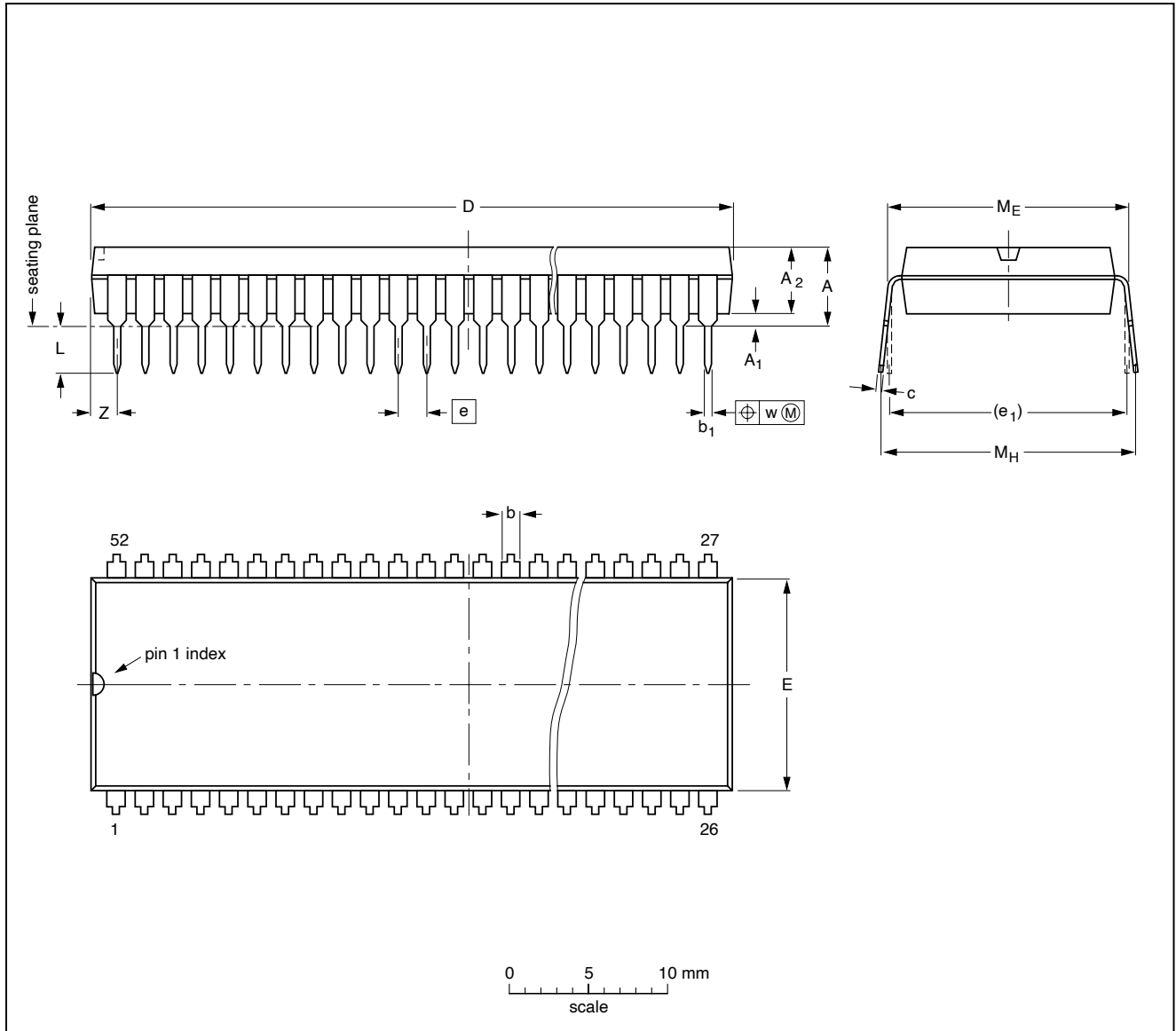
TV microcontrollers with Closed Captioning (CC) and On-Screen Display (OSD)

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25 PACKAGE OUTLINES

SDIP52: plastic shrink dual in-line package; 52 leads (600 mil)

SOT247-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A1 min. | A2 max. | b | b1 | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e1 | L | ME | MH | w | Z ⁽¹⁾ max. |
|------|--------|---------|---------|------------|--------------|--------------|------------------|------------------|-------|-------|------------|----------------|----------------|------|-----------------------|
| mm | 5.08 | 0.51 | 4.0 | 1.3 0.8 | 0.53 0.40 | 0.32 0.23 | 47.9 47.1 | 14.0 13.7 | 1.778 | 15.24 | 3.2 2.8 | 15.80 15.24 | 17.15 15.90 | 0.18 | 1.73 |

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

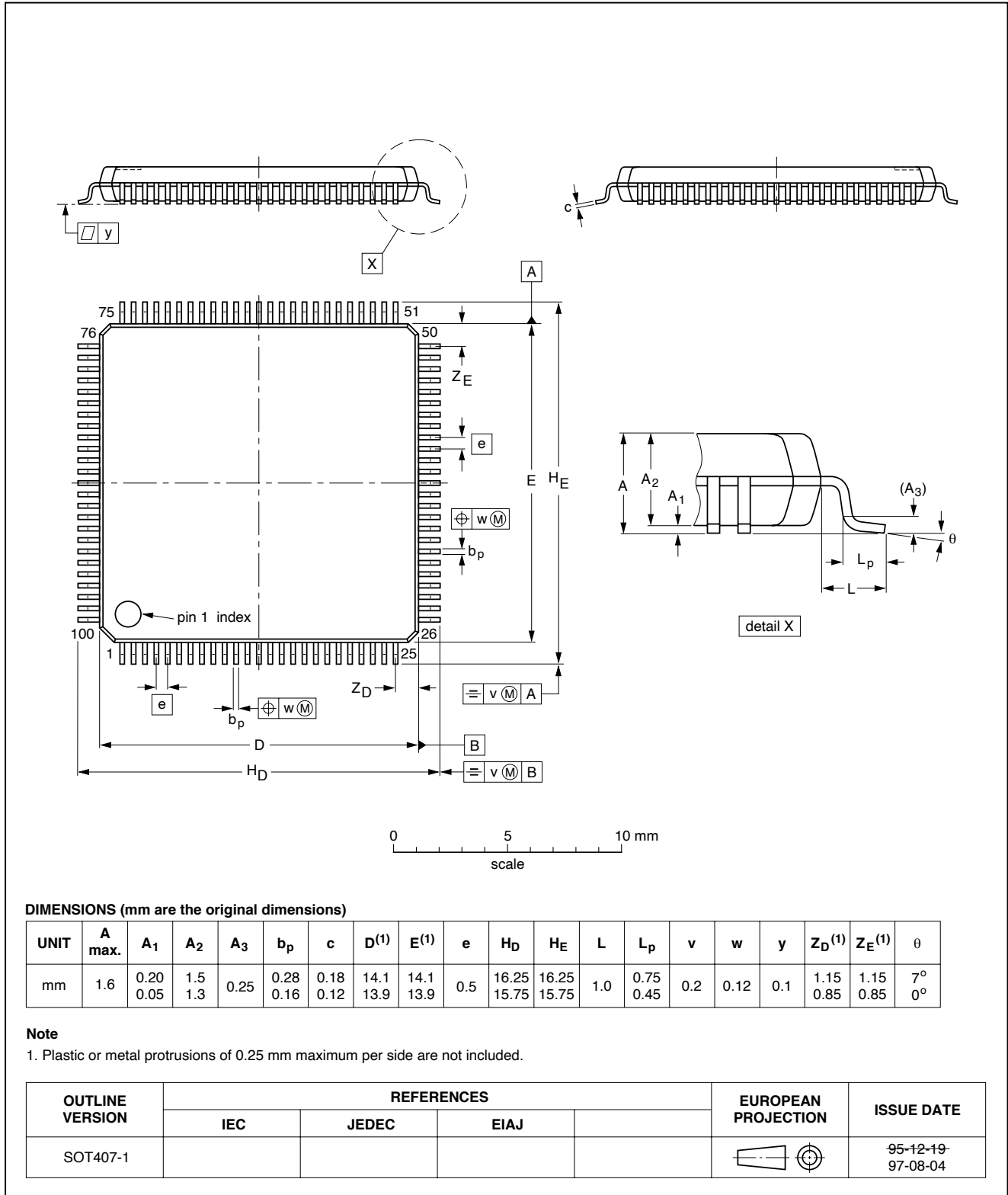
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|------|--|---------------------|---------------------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT247-1 | | | | | | 90-01-22 95-03-11 |

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LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm

SOT407-1



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26 SOLDERING

26.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

26.2 Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

26.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

26.4 Suitability of through-hole mount IC packages for dipping and wave soldering methods

| PACKAGE | SOLDERING METHOD | |
|---------------------------|------------------|-------------------------|
| | DIPPING | WAVE |
| DBS, DIP, HDIP, SDIP, SIL | suitable | suitable ⁽¹⁾ |

Note

- For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

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27 DEFINITIONS

| | |
|---|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

28 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

29 PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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NOTES

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