DESCRIPTION

PT2259 is an 8-pin 2-channel volume controller which utilizes CMOS technology and incorporates the I^2C interface control. The controller features an attenuation range of 0 to -79dB, low noise output, a high degree of stereo separation and requires only a small number of external components. PT2259 is an essential component for modern audio visual systems.

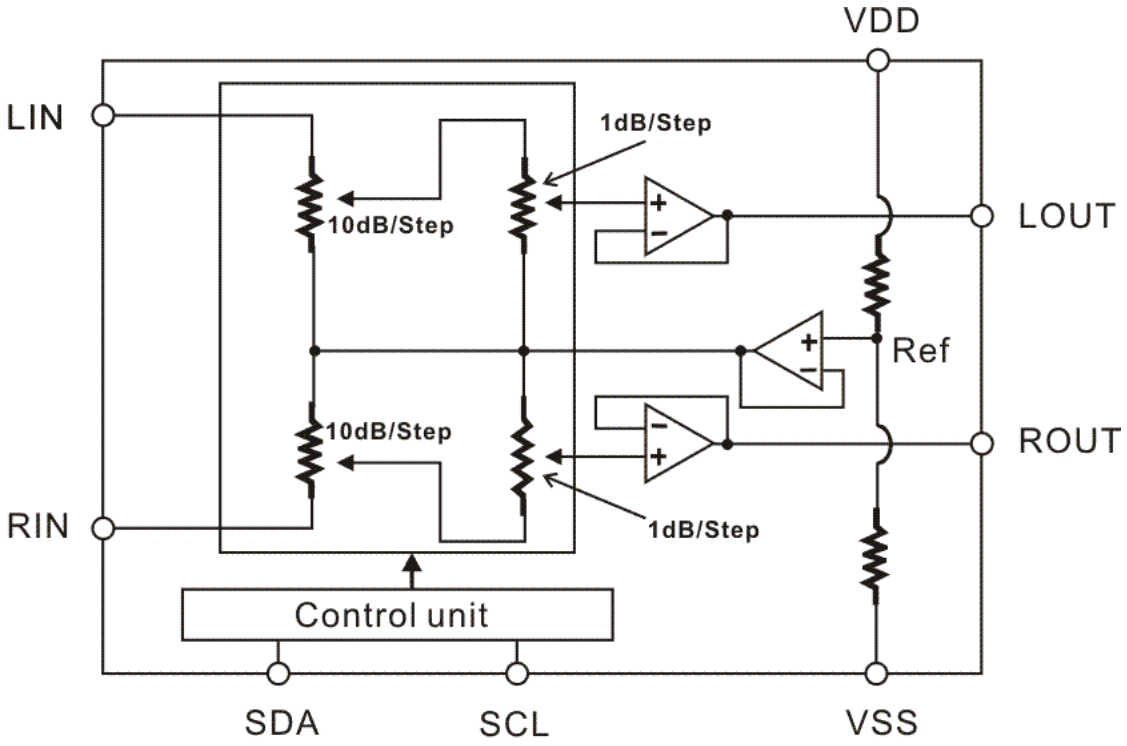
FEATURES

- Attenuation range: 0 to -79dB in 1dB steps
- Operating voltage: 4 to 10V
- Low power consumption
- Low signal noise: S/N > 100dB (A-weighting)
- Stereo separation > 100dB
- Requires few external components
- 2-channel volume individual adjust
- Available in 8 Pins DIP or SOP

APPLICATIONS

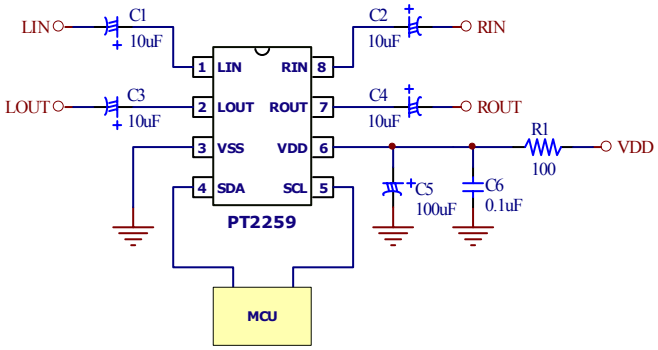
- Audio/visual surround sound systems
- Car audio systems
- Mini-compo systems
- Computer multi-media speakers
- Other audio applications

BLOCK DIAGRAM

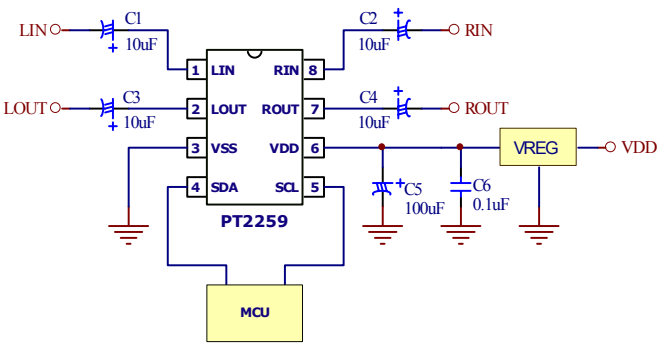


APPLICATION CIRCUIT

IMPROVE VDD NOISES REJECTION

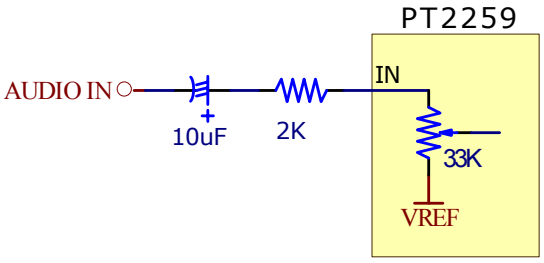


ADD a RC filter on the VDD path

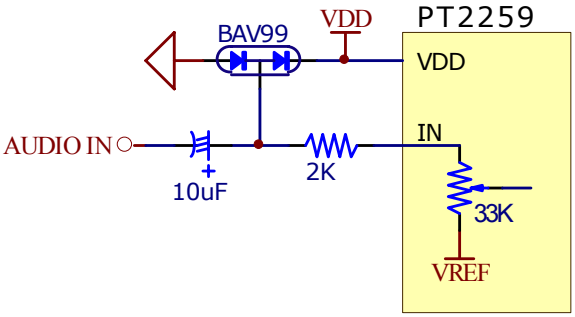


Use a regulated supply

IMPROVE INPUT ESD HANDLING CAPABILITY



ADD a Resistor on the input path

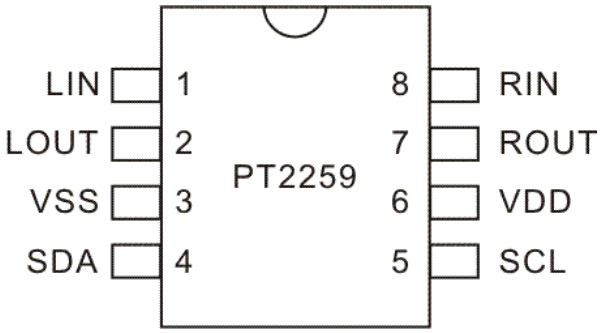


ADD a protection diode on the input path

ORDERING INFORMATION

Valid Part Number	Package Type	Top Code
PT2259	8 Pins, DIP, 300mil	PT2259
PT2259-S	8 Pins, SOP, 150mil	PT2259-S

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
LIN	I	Left Channel Input (capacitor coupled to input port)	1
LOUT	O	Left Channel Output (capacitor coupled to output port)	2
VSS	-	Ground	3
SDA	I	I^2C Data Input	4
SCL	I	I^2C Clock Input	5
VDD	-	Power Supply	6
ROUT	O	Right Channel Output (capacitor coupled to input port)	7
RIN	I	Right Input Channel (capacitor coupled to output port)	8

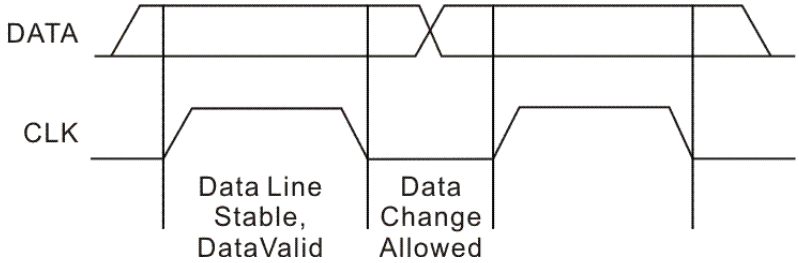
FUNCTIONAL DESCRIPTION

I²C BUS INTERFACE

In PT2259 the DATA and CLK make up the bus interface through which data is transmitted to and from the microprocessor.

DATA VALIDITY

Data on the DATA line is considered valid and stable only when the CLK signal is in the “high” state. In addition, the “high” and “low” states of the DATA line can change only when the CLK signal is in the “low” state. Please refer to the diagram below:

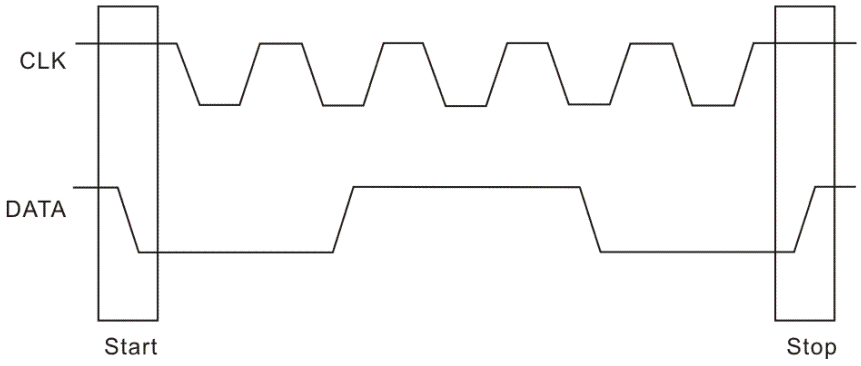


START AND STOP CONDITIONS

A start condition is activated when:
1. the CLK signal is set to “high”, and
2. the DATA signal shifts from “high” to “low”

A stop condition is activated when:
1. the CLK signal is set to “high”, and
2. the DATA signal shifts from “low” to “high”

Please refer to the timing diagram below:

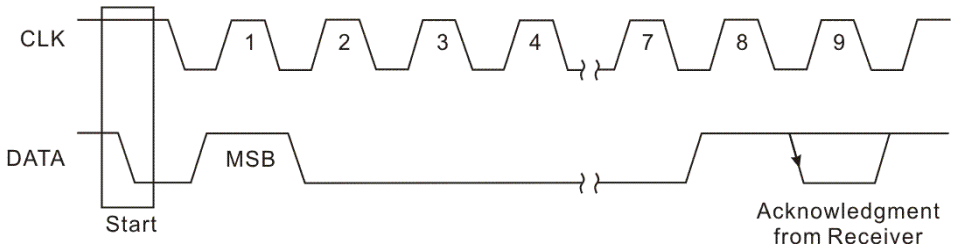


BYTE FORMAT

Every byte transmitted to the DATA line consists of 8 bits and each byte must be followed by an “acknowledge” bit. The MSB is transmitted first.

ACKNOWLEDGE SIGNAL

During the ninth clock pulse, the microprocessor puts a resistive “high” level on the DATA line. If the peripheral audio processor (PT2259) acknowledges, it will pull the DATA line from a “high” state to a “low” state during this acknowledge clock phase so that the DATA line is in a stable “low” state during this clock pulse. Please refer to the diagram below.



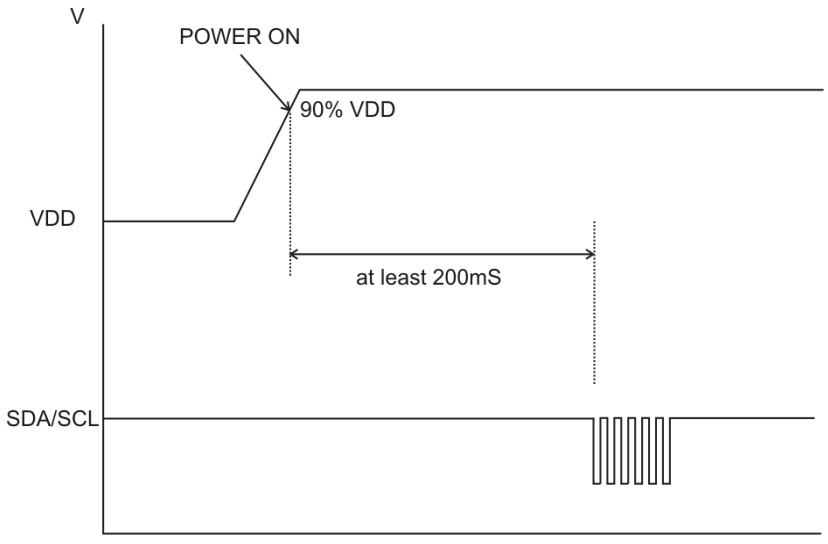
The audio processor that has been address (PT2259) must generate an “acknowledge” signal after receiving each byte or the DATA line will remain at the “high” level during the ninth clock pulse.

TRANSMISSION WITHOUT ACKNOWLEDGE

If you do not wish the audio processor (PT2259) to detect the “acknowledge” signal, a simpler microprocessor transmission method can be used: after PT2259 has received a byte wait for one clock pulse and do not acknowledge it. If this approach is used, however, there is a greater chance for faulty operations to occur and noise immunity will be decreased.

I^2C START TIME

When PT2259 is powered on, a short period must elapse before voltage becomes stable. After the power is turned on, PT2259 must wait at least 200ms before it is able to send an I^2C control signal otherwise control efficacy and normal operation will be comprised. Please refer to the diagram below:

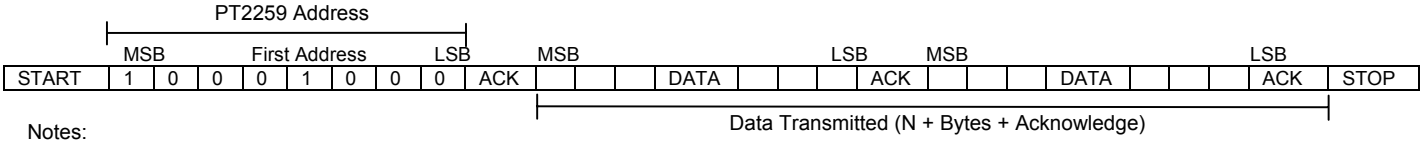


INTERFACE PROTOCOL

The interface protocol consists of the following:

1. a start condition
2. the PT2259 address byte followed by an “acknowledge” signal
3. a data sequence (n-bytes and an “acknowledge” signal)
4. a stop condition

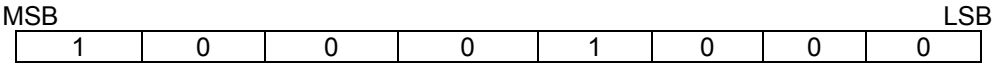
Please refer to the following diagram:



Notes:
1. ACK= Acknowledge
2. Max Clock Speed = 100K BITS/S

SOFTWARE SPECIFICATIONS

PT2259 address is shown below



DATA BYTES DESCRIPTION

FUNCTION BITS

MSB							LSB	Function
1	1	0	1	A3	A2	A1	A0	2-channel, -1dB/step
1	1	1	0	0	B2	B1	B0	2-channel, -10db/step
1	0	1	0	A3	A2	A1	A0	Left channel, -1db/step
1	0	1	1	0	B2	B1	B0	Left channel, -10dB/step
0	0	1	0	A3	A2	A1	A0	Right channel, -1dB/step
0	0	1	1	0	B2	B1	B0	Right channel, -10dB/step
1	1	1	1	0	0	0	0	Clear register
0	1	1	1	0	1	C1	C0	Mute select

ATTENUATION UNIT BITS

A3	A2/B2	A1/B1	A0/B0	Attenuation (dB)
0	0	0	0	0/0
0	0	0	1	-1/-10
0	0	1	0	-2/-20
0	0	1	1	-3/-30
0	1	0	0	-4/-40
0	1	0	1	-5/-50
0	1	1	0	-6/-60
0	1	1	1	-7/-70
1	0	0	0	-8/
1	0	0	1	-9/

MUTE FUNCTION BITS

C1	C0	Function
0	0	Mute OFF
0	1	Right channel mute ON
1	0	Left channel mute ON
1	1	Left and right channel mute ON

PT2259 I²C CODE SEQUENCE

User must following I²C code sequence describe in this section in order to ensure proper operation under various operation voltage. If any register doesn't given an initial value, or code sequence is not following the instruction, the PT2259 is possible out of control. Please refer to the following instruction.

1st, clear the volume register

Start	0x88	0xF0	Stop

0x88: PT2259 chip address
0xF0: Clear register
(This procedure only needs perform once after power on.)

2nd, give all register an initial value

Start	0x88	0x74	0xE2	0xD0	Stop

0x88: PT2259 chip address
0x74: All channels mute off
0xE2: 2-channels -20dB
0xD0: 2-channels -0dB
(1dB code must follow a 10dB code and not be interrupted)

3rd, follow the code sequence 2nd to setting functions.

Start	0x88	0x74	0xE2	0xD0	Stop

Set volume to -20dB, all channels mute off

Start	0x88	0x74	0xE1	0xD9	Stop

Set volume to -19dB, all channels mute off

Start	0x88	0x77	0xE1	0xD9	Stop

Set volume to -19dB, all channels muted

Start	0x88	0x74	0x31	0x29	Stop

Set R-CH volume=-19dB, all mute=off

WARNING! THESE TRANSMISSION METHODS ARE PROHIBITED.

Only a 10dB attenuation value:

Start	0x88	0xE4	Stop
		-40dB	

Only a 1dB attenuation value:

Start	0x88	0xD2	Stop
		-2dB	

Other code occupied in between the 10dB and 1dB code.

Start	0x88	0xD2	0x22	0xE4	Stop
		-2dB	R-CH -2dB	-40dB	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	12	V
Operating Temperature	Topr	-40 ~ +85	°C
Storage Temperature	Tstg	-65 ~ +150	°C
Input Voltage	Vi	-0.3 ~ Vcc + 0.3	V

ELECTRICAL CHARACTERISTICS

(Conditions: Vcc=9V, Vi=1Vrms, f=1KHz, Temp=27°C)

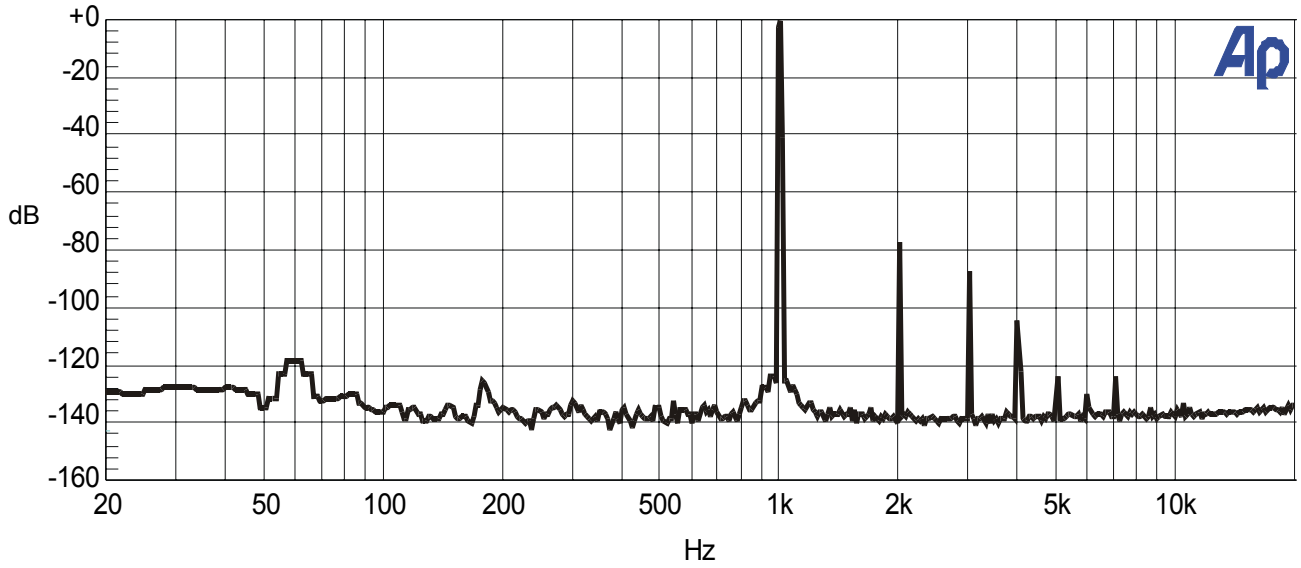
Parameter	Symbol	Testing Conditions		Min.	Typ.	Max.	Unit
Operating Voltage	Vcc			4	9	10	V
Operating Current	Icc	Vcc=9V, Vi=0V		-	2.5	3	mA
Volume Attenuation Range	ARANGE	Minimum attenuation		-	0	-	dB
		Maximum attenuation		-	-79	-	
Attenuation Step	ASTEP	-		-	1	-	dB
Attenuation Step Gain Error	GERR	-		-	0.5	-	dB
Interchannel Attenuation Gain Error	CERR	-		-	0.5	-	dB
Maximum Output Voltage	Vomax	Vcc=9V, freq=1KHz, Volume Att.=0dB, Rload=50KΩ, THD<1%		2.0	2.3	2.5	Vrms
Total Harmonic Distortion	THD	f=1KHz, Vol.Att.=0dB, A-weight Rload=50KΩ	Vout=2Vrms	-	0.07	0.09	
			Vout=200mVrms	-	0.003	0.005	%
Noise Output	NO	Vin=GND, Mute=OFF, Volume Att = 0dB, A-weighted		-	2	3	μVrms
Signal-to-Noise Ratio	SNR	Vin=1Vrms, Att.=0dB	No-weighted	95	100	103	dB
			A-weighted	110	120	125	
Channel Separation	CS	Vin=2.5Vrms, freq.=1KHz, Volume Att.=0dB		100	120	125	dB
Mute	MUTE	Vin=2.5Vrms, freq.=1KHz, Vol. Att.=0dB, A-weighted		90	95	97	dB
Frequency Response	FR	Vin=1Vrms, Volume Att.=-10dB		-	1	1.3	MHz
Input Impedance	Rin	f=1KHz		-	33	-	KΩ
Output Impedance	Rout	f=1KHz, Vout=100mVrms		-	6	-	Ω
Minimum Load Resistance	Rload	VDD=9V, Vo=2Vrms, THD<1%		6	-	-	KΩ

I²C BUS SECTION ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VIH	Bus High Input Level	-	3.5	-	-	V
VIL	Bus Low Input Level	-	-	-	0.8	V

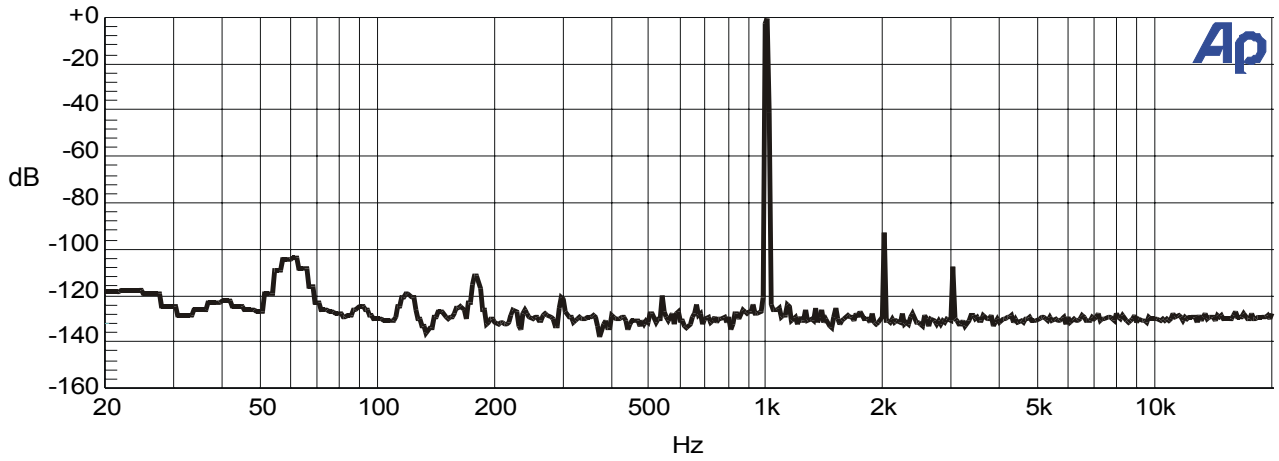
PT2259 THD - FAST FOURIER TRANSFORM (FFT) ANALYSIS 1

(Conditions: Rload=10K, Volume Att=0dB, Vcc=9V, Output Level=1Vrms)



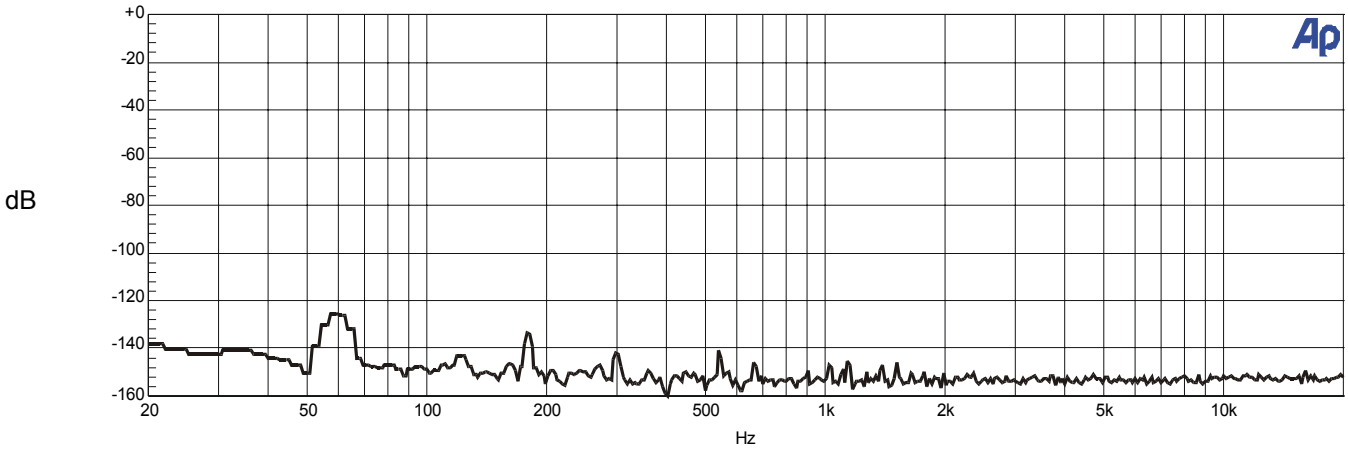
PT2259 THD - FAST FOURIER TRANSFORM (FFT) ANALYSIS 2

(Conditions: Rload=10K, Volume Att=0dB, Vcc=9V, Output Level=200mVrms)



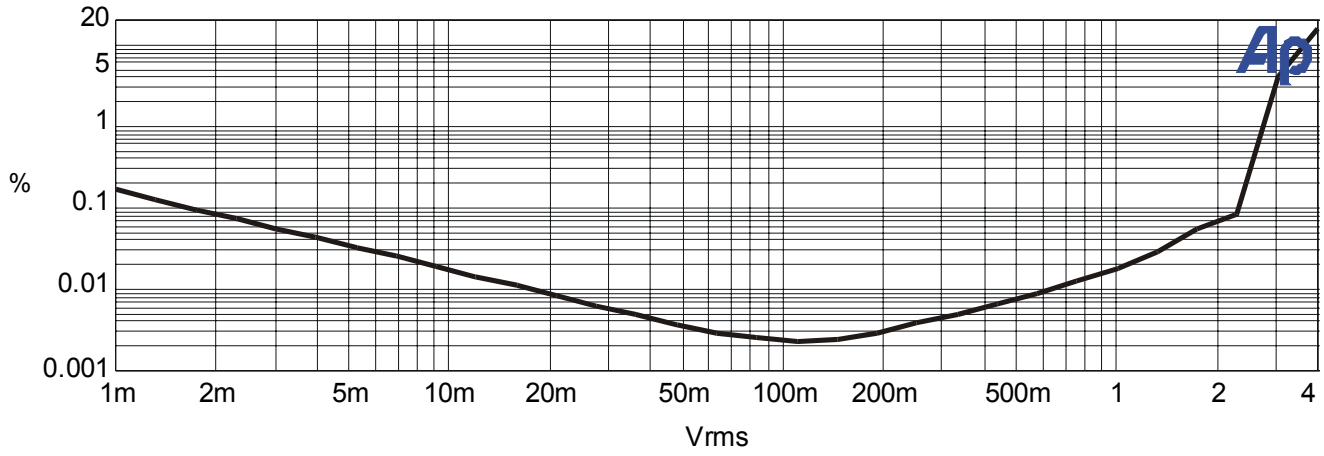
PT2259 NOISE FLOOR - FAST FOURIER TRANSFORM (FFT) ANALYSIS 3

(Conditions: Rload=10K, Volume Att=0dB, Vcc=9V, Vin=GND)



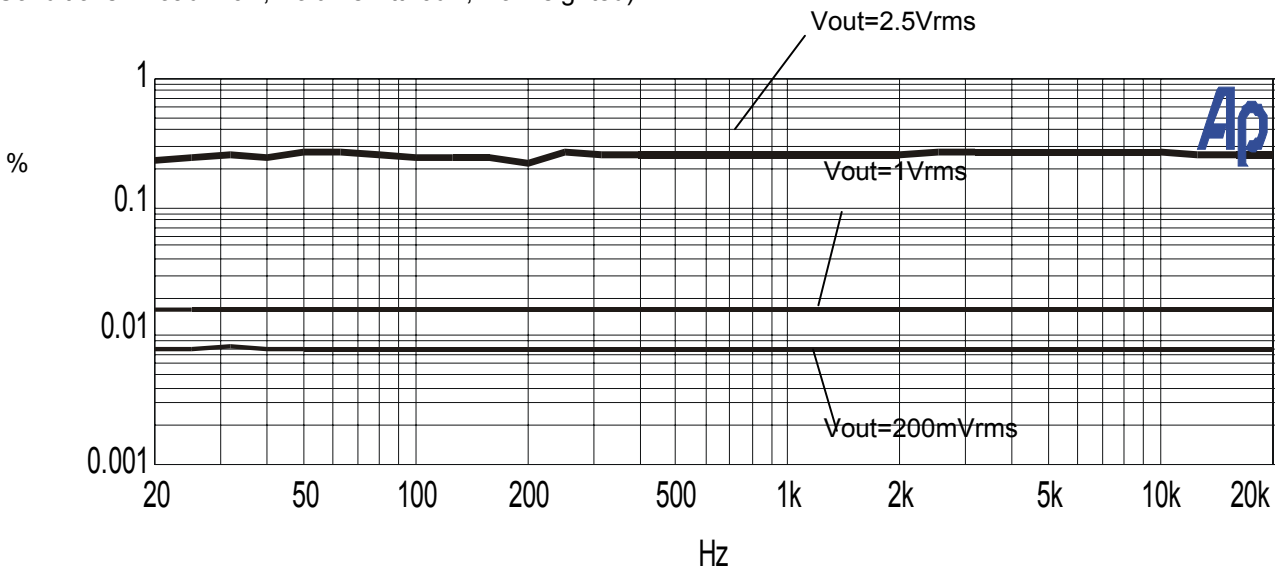
PT2259 THD VS. OUTPUT LEVEL

(Conditions: Rload=10K, Volume Att=0dB, Vcc=9V, f=1KHz, A-weighted)



PT2259 THD VS. FREQUENCY RESPONSE AT VARIOUS OUTPUT LEVELS

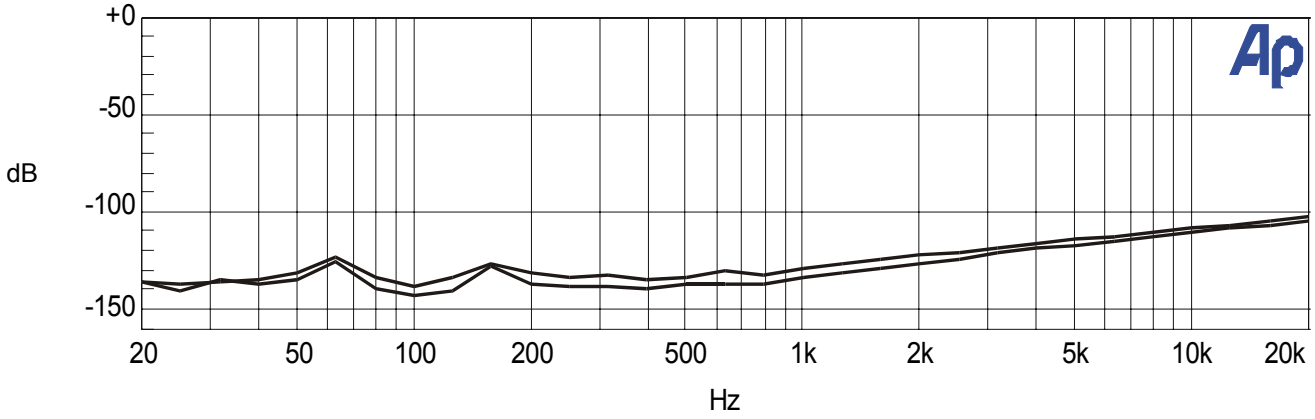
(Conditions: Rload=10K, Volume Att=0dB, No-weighted)



Note: from top to bottom: Vout = 2.5Vrms, 1Vrms = 200mVrms

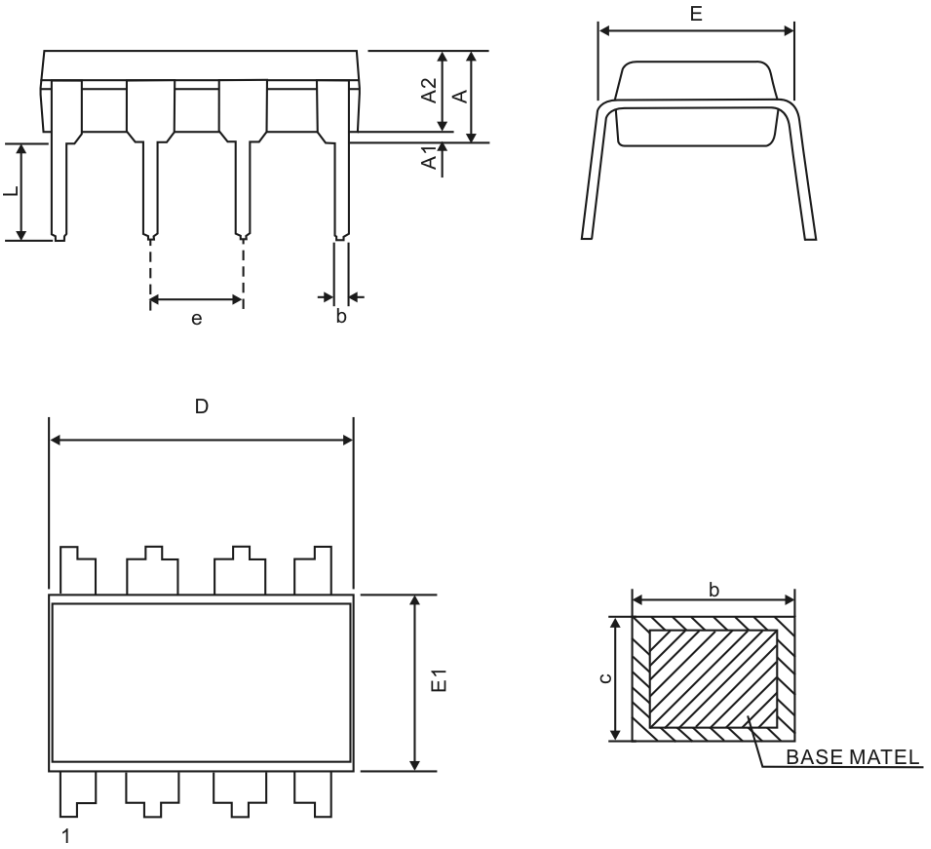
PT2259 INTERCHANNEL CROSSTALK

(Conditions: Rload=10K, Volume Att=0dB)



PACKAGING INFORMATION

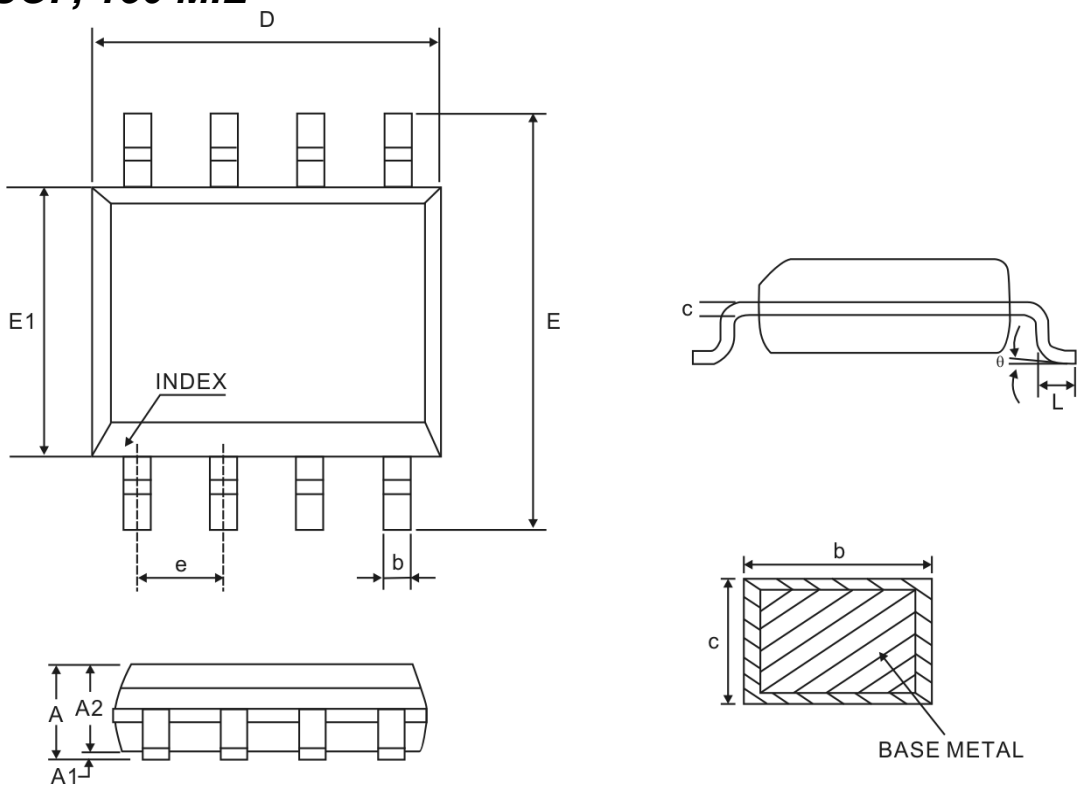
8-PIN, DIP, 300 MIL



Symbol	Dimensions (MM)		
	Min.	Nom.	Max.
A	-	-	4.80
A1	0.50	-	-
A2	3.10	3.30	3.50
b	0.38	-	0.55
c	0.21	-	0.35
e		2.54 BSC	
D	9.10	9.20	9.30
E	7.62	7.87	8.25
E1	6.25	6.35	6.45
L	2.92	3.30	3.81

Note: Refer to JEDEC MS-001 BA

8-PIN, SOP, 150 MIL



Symbol	Dimensions (MM)		
	Min.	Nom.	Max.
A	1.35	1.60	1.77
A1	0.08	0.15	0.28
A2	1.20	1.40	1.65
b	0.33	-	0.51
c	0.17	-	0.26
e	1.27 BSC		
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
L	0.38	0.60	1.27
θ	0°	-	8°

Note: Refer to JEDEC MS-012 AA

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.
PTC cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a PTC product. No circuit patent licenses are implied.

Princeton Technology Corp.
2F, 233-1, Baociao Road,
Sindian, Taipei 23145, Taiwan
Tel: 886-2-66296288
Fax: 886-2-29174598
http://www.princeton.com.tw