LC7515

3021B

T-77-21

CMOS IC

Automatic Music Selector (up to 5 Selections) for Tape Recorders

©11698

The LC7515 is a single-chip CMOS IC designed to automatically select your desired music up to 5 selections preceding or following the selection being played.

Applications
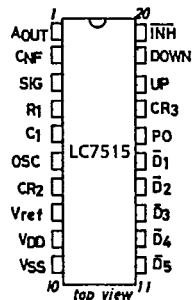- Radio-cassette recorders, cassette decks, car stereos

Features
- Preamp, unrecorded section sense unit, and automatic music selection (up to 5 selections) logic unit are built in.
- Unrecorded section sense time and recorded section sense time are set independently by external CR, so that stable operation is made possible against pulse noise in unrecorded section and sound cut in recorded section.
- For programming the number of selections, serial set (endless) mode in up/down direction is available.
- It is possible to direct drive 5 LEDs for displaying the number of programmed selections.
- At the time of completion of music selection and power application, no program mode takes place. Automatic 1-selection programming is also enabled by external circuit. (Refer to Sample Application Circuits 3,4.)
- Meets the requirements for deck mechanisms of 2 types (1. plunger OFF during music selection, 2. plunger ON during music selection).
- Input sensitivity : -52dBm typ $(f=10$kHz$)$
- Wide operating voltage range $(V_{DD}=5.0$ to 11.0V$)$ and small current dissipation $(I_{DD}\leqq 2.5$mA$)$
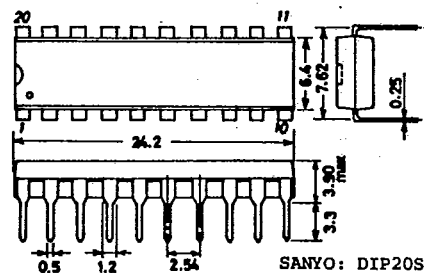- Package : DIP20S (slim type)

Absolute Maximum Ratings at $Ta=25°C, V_{SS}=0V$

		Pin Name	Pin No.			unit
Maximum Supply Voltage	V_{DD} max	V_{DD}	9		$V_{DD}-0.3$ to $V_{SS}+12$	V
Reference Voltage	Vref	Vref	8	$Vref\leqq V_{DD}$	$V_{SS}-0.3$ to $V_{SS}+11$	V
Input Voltage	V_{IN}	C_{NF},SIG,UP, DOWN,$\overline{INH}$	2,3,18, 19,20		$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Output Voltage	V_{OUT}	$A_{OUT},R_1,C_1,$ OSC,CR_2,PO, $CR_3,\overline{D_1}$ to $\overline{D_5}$	1,4,5,6, 7,16,17, 15 to 11	Output transistor off	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Output Current	I_{OUT}	$\overline{D_1}$ to $\overline{D_5}$	15 to 11		30	mA
Allowable Power Dissipation	Pd max			$Ta\leqq 75°C$	300	mW
Operating Temperature	Topg				-30 to $+75$	°C
Storage Temperature	Tstg				-40 to $+125$	°C

Pin Assignment

Pin layout (top view), LC7515:

Left side (pins 1–10): A_{OUT} (1), C_{NF}, SIG, R1, C1, OSC, CR2, Vref, VDD, VSS (10)

Right side (pins 20–11): $\overline{INH}$ (20), DOWN, UP, CR3, PO, $\overline{D_1}$, $\overline{D_2}$, $\overline{D_3}$, $\overline{D_4}$, $\overline{D_5}$ (11)

Case Outline 3021B-D20SIC (unit : mm)

6.4 7.62 0.25 24.2 3.3 3.90 0.5 1.2 2.54

SANYO: DIP20S

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Allowable Operating Conditions at Ta = 25°C, Vss = 0V

		Pin Name	Pin No.		min	typ	max	unit
Supply Voltage	V_{DD}	V_{DD}	9		5		11	V
Reference Voltage	Vref	Vref	8	Vref $\leq V_{DD}$	4		11	V
Input 'H'-Level Voltage	V_{IH}	CR_3, UP, DOWN, $\overline{INH}$	17,18 19,20		$0.8V_{DD}$		V_{DD}	V
Input 'L'-Level Voltage	V_{IL}	UP, DOWN, $\overline{INH}$	18,19,20		V_{SS}		$0.2V_{DD}$	V
External Capacitance	$C_{EXT(1)}$	C_1	5			1.0	2.2	µF
	$C_{EXT(2)}$	CR_2, CR_3	7,17			1.0	10	µF
	$C_{EXT(3)}$	OSC	6			0.01	2.2	µF
	$C_{EXT(4)}$	C_{NF}	2		0.47	1.0	1.2	µF
	$C_{EXT(5)}$	A_{OUT}-C_{NF}	1-2		33	36	39	pF
	$C_{EXT(6)}$	A_{OUT}	1		470	1000	1500	pF
	$C_{EXT(7)}$	SIG	3			0.1	2.2	µF
External Resistance	$R_{EXT(1)}$	R_1	4		0	100	430	kΩ
	$R_{EXT(2)}$	CR_2	7		0.68	100	430	kΩ
	$R_{EXT(3)}$	CR_3	17		1	100	240	kΩ
	$R_{EXT(4)}$	OSC	6		0.68	100	510	kΩ
	$R_{EXT(5)}$	C_1	5		0.68	1	10	kΩ
	$R_{EXT(6)}$	A_{OUT}-C_{NF}	1-2		180	240	300	kΩ
	$R_{EXT(7)}$	C_{NF}	2		0.51	1	3	kΩ

Electrical Characteristics at Ta = 25°C, Vss = 0V, V_{DD} = Vref = 5 to 9V

					min	typ	max	unit
Input Threshold Voltage	V_t	SIG	3	GAIN 48dB, V_{DD}=5V, f=10kHz	−55 (1.38)	−52 (1.95)	−49 (2.75)	dB mV
	$V_{tL}(1)$	CR_3	17	V_{DD}=5 to 6V	$0.25V_{DD}$		$0.7V_{DD}$	V
	V_{tH}	C_1, CR_2	5,7	V_{DD}=5 to 6V	$0.5Vref$ −250		$0.5Vref$ +250	mV
	$V_{tL}(2)$	C_1, CR_2	5,7	V_{DD}=5 to 6V	$3/8Vref$ −250		$3/8Vref$ +250	mV
Output 'H'-Level Voltage	V_{OH}	PO, CR_3	16,17	I_{OH} = −10mA	V_{DD}−2.5		V_{DD}	V
Output 'L'-Level Voltage	$V_{OL}(1)$	$\overline{D_1}$ to $\overline{D_5}$	15 to 11	I_{OL}=25mA	V_{SS}		V_{SS}+1.9	V
	$V_{OL}(2)$	PO	16	I_{OL}=10mA	V_{SS}		V_{SS}+2.5	V
Output OFF Leakage Current	$I_{OFF}(1)$	R_1, OSC, CR_3	4,6,17	V_{OUT}=V_{SS}	−5		0	µA
	$I_{OFF}(2)$	C_1, CR_2	5,7	V_{OUT}=V_{DD}	0		5	µA
	$I_{OFF}(3)$	$\overline{D_1}$ to $\overline{D_5}$	15 to 11	V_{OUT}=V_{DD}	0		5	µA
Output ON Resistance	$R_{ON}(1)$	C_1, CR_2	5,7	V_{DD}=5V, V_{OUT}=V_{DD}	0		300	Ω
	$R_{ON}(2)$	R_1	4	V_{DD}=5V, V_{OUT}=V_{SS}	0		1	kΩ
Input Impedance	Z_{IN}	SIG	3	C_{NF}: AC grounded, f=10kHz	100	170	260	kΩ
Input 'H'-Level Current	$I_{IH}(1)$	SIG	3	Vref=V_{DD}=5V, V_{IN}=V_{DD}	11.5	19.5	32.5	µA
	$I_{IH}(2)$	UP, DOWN	18,19	V_{DD}=5V, V_{IN}=V_{DD}	10	50	100	µA
Input 'L'-Level Current	$I_{IL}(1)$	SIG	3	Vref=V_{DD}=5V, V_{IN}=V_{SS}	−16	−9.5	−5	µA
Input Leakage Current	$I_{IH}(3)$	$\overline{INH}$	20	V_{IN}=V_{DD}	0		5	µA
	$I_{IL}(2)$	$\overline{INH}$	20	V_{IN}=V_{SS}	−5		0	µA
Supply Current	Iref	Vref	8	CR_3, OSC=V_{DD}, C_{NF}, $\overline{INH}$=V_{SS}, others: open	0		3	mA
	I_{DD}	V_{DD}	9	CR_3, OSC, Vref=V_{DD}, C_{NF}, $\overline{INH}$=V_{SS}, others: open	0		2.5	mA

(Note) Current direction (+, no sign : Flowing into device, − : Flowing out of device)
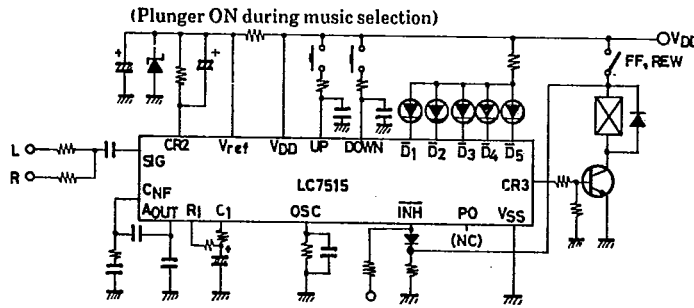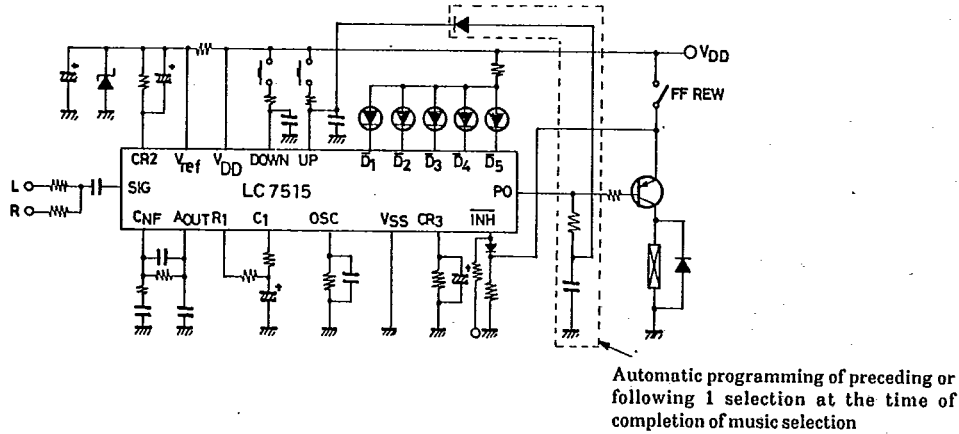
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Equivalent Circuit Block Diagram

Sample Application Circuit 1

(Plunger ON during music selection)
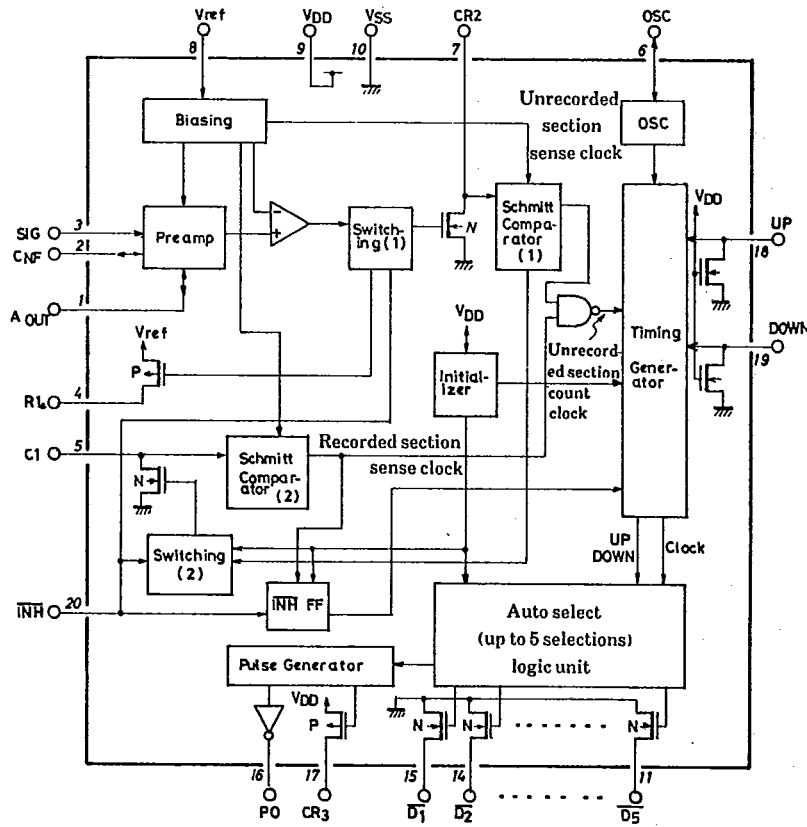
Sample Application Circuit 2

(Plunger OFF during music selection)
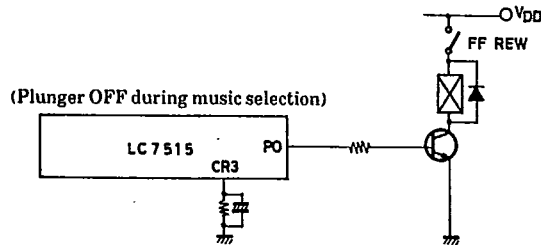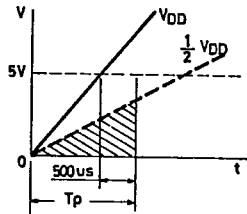
Sample Application Circuit 3 : Automatic programming of preceding or following 1 selection at the time of application of power or completion of music selection (Plunger ON during music selection)


Automatic programming of preceding or following 1 selection at the time of completion of music selection

In this application, V_{DD} and Vref rise modes must meet the following condition.

Vref level must not exceed $1/2 V_{DD}$ during T_P period.

※ If V_{DD} and Vref rise modes are $V_{DD} \simeq$ Vref or $V_{DD} =$ Vref, Sample Application Circuit 4 shown below can be used for automatic programming of preceding or following 1 selection.

Sample Application Circuit 4 : Automatic programming of preceding or following 1 selection at the time of application of power or completion of music selection (Plunger ON during music selection)

Automatic programming of preceding or following 1 selection at the time of completion of music selection

Automatic programming of preceding or following 1 selection at the time of application of power
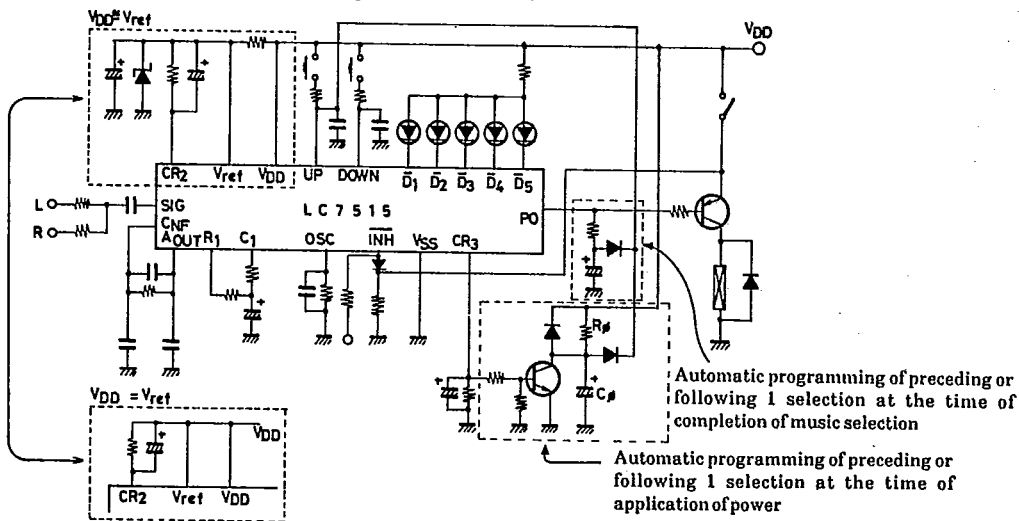
• Condition
V_{DD} rise time must be much shorter than $R\phi \cdot C\phi$ time constant.

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Operation Description

(1) Application of power

Initialization at the time of application of power is made automatically by the initialization circuit, that is to say, the undermentioned $\overline{INH}$ F·F is set and the timing generator and auto select logic unit are initialized. (Refer to Block Diagram.)

(2) Music selection start

Music selection is started by changing-over the level of $\overline{INH}$ pin from "L" to "H" while power supply is applied.

In order that ① when music selection is started with any unrecorded section, this section is prevented from being sensed and ② when the REW music selection is started with any head of music (recorded section), the unrecorded section immediately following this head is prevented from being sensed, the unrecorded section sense unit functions as follows:

In either mode of these two where music selection is started, C_1 is discharged and the $\overline{INH}$ F·F is set. Therefore, for ①, audio signal is input to SIG pin and P channel transistor at R_1 pin is turned ON and C_1 is charged up through external resistor R_1. When the charged-up voltage exceeds the check level of the Schmitt comparator at C_1 pin, the output (recorded section sense clock) of the Schmitt comparator at C_1 pin is set at "H" level, the $\overline{INH}$ F·F is reset, and unrecorded section sense operation in (3) is started. (Refer to period Ⓐ of Timing Chart.)

For ②, since music selection is started with the head of music (recorded section), C_1 is charged up immediately. However, next unrecorded section comes before C_1 charge-up voltage reaches the check level of the Schmitt comparator during the period of $C_1 \cdot R_1$ time constant and C_1 is discharged by the built-in N channel transistor.

Thus, the $\overline{INH}$ F·F is not reset and the same operation as in ① occurs thereafter and the unrecorded section sense operation is entered.

When releasing inhibit mode with the mechanism-coupled switch, some delay between switch ON/OFF signal and $\overline{INH}$ pin input signal may be required. With the Schmitt inverter built in INH· pin, this delay can be caused easily with an external integrator.

(3) Unrecorded section sense operation

When audio signal is input from SIG pin, N channel transistor at CR_2 pin is turned ON and CR_2 pin is set at "L" level. External capacitor C_2 is charged up. When an unrecorded section is reached and audio signal disappears, N channel transistor at CR_2 pin is turned OFF. Capacitor C_2 starts discharging through external resistor R_2. When CR_2 pin voltage rises and exceeds the check level of the built-in Schmitt comparator, Schmitt comparator output (unrecorded section sense clock) changes from "H" level to "L" level and the unrecorded section is counted. (Refer to Ⓐ → Ⓑ of Time Chart.)

As a precaution to be taken in application, it should be noted that the following phenomenon may occur. If pulse noise exists during the unrecorded section sense operation, N channel transistor at CR_2 pin is turned ON, external capacitor is charged up instantaneously, and then the set-up period of discharge time is needed, and thereby the unrecorded section sense operation goes imperfect. To avoid this phenomenon, the unrecorded section sense time is improved by inserting resistor R_2' between CR_2 pin and external C_2, R_2.

Improvement in unrecorded section sense time
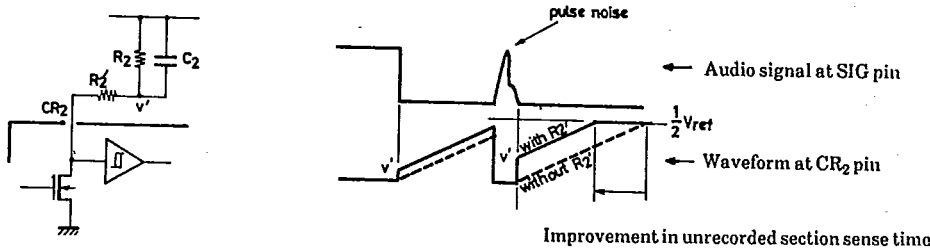
Unrecorded section sense time t can be calculated by the following formula.

$$t = C_2 R_2 \ln \left(\frac{1}{1 - \frac{(1/2 V_{ref} \pm 250mV)}{V_{ref}}} \right)$$

±250mV : Schmitt comparator offset

$$t(typ) = C_2 R_2 \ln 2 = 0.693 C_2 R_2$$

With no offset of Schmitt comparator
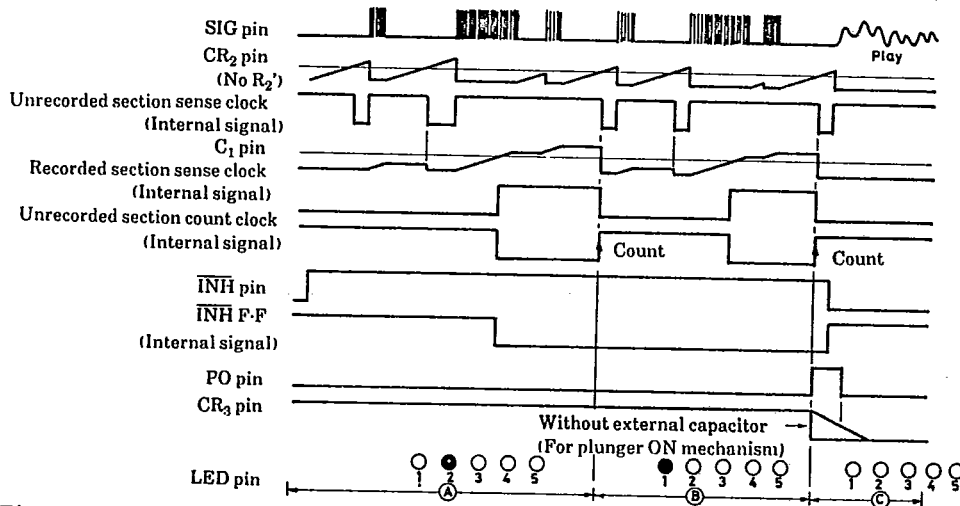
C_2 : External capacitor capacitance (F)

R_2 : External resistor resistance (Ω)

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(4) Recorded section sense operation

When an unrecorded section is sensed, external capacitor at C_1 pin is discharged in readiness for next recorded section sense operation and Schmitt comparator output (recorded section sense clock) at C_1 pin is set at "L" level.

The unrecorded section count clock is a NAND output of recorded section sense clock and unrecorded section sense clock and unrecorded section count operation is performed only when unrecorded section count clock is changed-over from "L" level to "H" level. Therefore, when recorded section sense clock is set at "L" level, unrecorded section count clock remains at "H" level regardless of unrecorded section sense clock mode and unrecorded section count operation is stopped. This mode remains until C_1 is charged up and Schmitt comparator output at C_1 pin is set at "H" level after the continuation of recorded mode for the period of time fixed by C_1, R_1. When recorded section sense clock is set at "H" level at the time unrecorded section sense clock is at "H" level, unrecorded section sense clock is set at "L" level and unrecorded section count standby mode takes place. When next unrecorded section is sensed, count operation is performed. As a result, pulse noise existing within the period of time fixed by C_1, R_1 is not identified as a recorded mode and unrecorded section which follows noise is not counted. (Refer to period Ⓑ of Pulse Noise Reject Operation Time Chart.) C_1 is discharged each time unrecorded section is sensed, so if the pulse noise period is shorter than the unrecorded section sense time fixed by C_2, R_2, C_1 is not charged up and pulse noise can be rejected, no matter how many times pulse noise occurs. Operations of ③ to ④ are repeated thereafter.

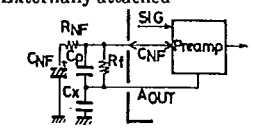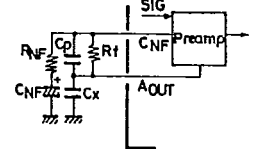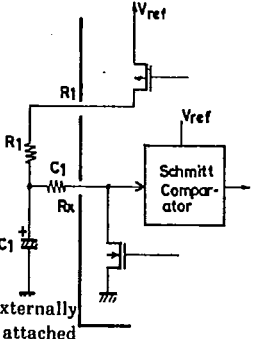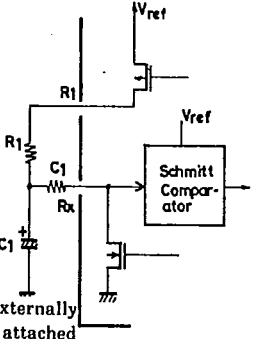**Unrecorded Section Count Operation Timing Chart**
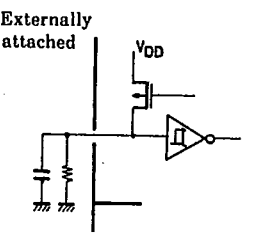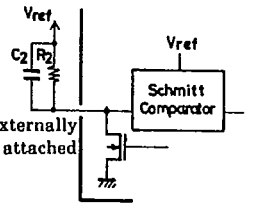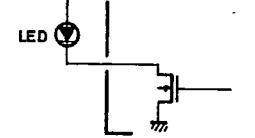
Pin Description

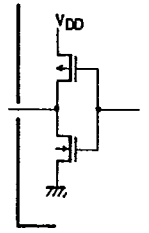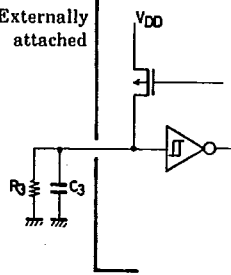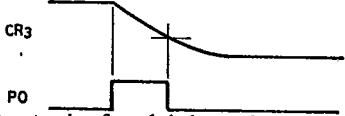| Pin Name	Pin No.	Input/Output	Pin Description
V_{DD} V_{SS}	9 10		· Pin for applying power $V_{SS}=0V, V_{DD}=5.0$ to $11.0V$
Vref	8		· Fixes check level of comparator, Schmitt comparator inside IC and supplies bias voltage of preamp. · Source power supply for P channel open drain transistor at R_1 pin · To secure accurate music select operation, voltage on this pin must be stabilized with Zener diode, etc. connected externally.
SIG	3	R L Cs Preamp Externally attached	· Input pin for unrecorded section sense audio signal · Preamp (input impedance $150k\Omega$ typ.) is built in and input sensitivity is $-52dBm$ (typ.). · Biased 3/8Vref (typ.) at pin open mode and used with capacitor coupling
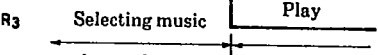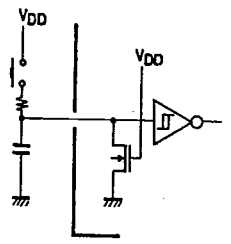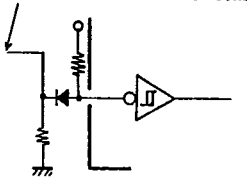
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Pin Name	Pin No.	Input/Output	Pin Description
C_{NF}	2	Externally attached	· Pin for setting preamp gain. Used for AC amp by connecting C, R across this pin and GND. Use capacitor with less leak current. · Biased 3/8Vref (typ.) at pin open mode
A_{OUT}	1		· Pin for setting preamp gain. Used with C, R connected across this pin and C_{NF}. · Pin for setting preamp attenuation at high frequencies. Used with C connected across this pin and GND.
R_1	4		· Pin for connecting external resistor which forms recorded section sense integrator · By connecting high resistor across this pin and C_1, C_1 is charged up through this resistor while being in recorded section. (Note) Recorded section sense time differs according to high input or low input. · P channel open drain
C_1	5	Externally attached	· Pin for connecting external capacitor which forms recorded section sense integrator · With built-in Schmitt comparator, recorded section sense operation is performed when pin voltage exceeds 1/2Vref. · Each time unrecorded section is sensed, capacitor is discharged, so recorded section sense integral action is repeated and pulse noise in unrecorded section is rejected. · To prevent latch-up, R_X is recommended.
OSC	6	Externally attached	· Pin for external CR for oscillator needed to operate internal logic unit. · Oscillation occurs only at the time of counting unrecorded section or changing program, and no oscillation occurs at the time of other than these operations. · Response time elapsing until program is changed after program switch (UP or DOWN) is turned ON is 3 times (3×Tosc) as long as oscillation cycle (Tosc). · By increasing CR time constant, program SW chattering can be rejected.
CR_2	7	Externally attached	· Pin for external CR which set unrecorded section sense time · With built-in Schmitt comparator, unrecorded section sense operation is performed when pin voltage exceeds 1/2Vref. · Unrecorded section sense time (t) is calculated by the following formula. $t \text{(typ.)} = 0.693\, C_2\, R_2$ C_2 : External capacitor capacitance (F) R_2 : External resistor resistance (Ω)
$\overline{D_1}$ $\overline{D_2}$ $\overline{D_3}$ $\overline{D_4}$	15 14 13 12	LED	· Output pin for LED driver for displaying programmed number of selections · N channel open drain output

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Continued from preceding page.

Pin Name	Pin No.	Input/Output	Pin Description
PO	16		· Pin for outputting positive pulse after completion of music selection. Pulse width depends on time constant of CR externally attached to CR₃ pin. · CMOS complementary output
CR₃	17		· Pin for external CR which fix output pulse width at Po pin · Input/output pin with built-in Schmitt type inverter · Output pin for driving plunger-ON mechanism (during music selection) at no program mode at the time of completion of music selection and application of power In this case, resistor only is connected and no capacitor is used. (Refer to Sample Application Circuit 1.) · When number of selections is programmed, high level is output. · P channel open drain output
UP	18		· Input pin for setting number-of-selections program in upward direction $\rightarrow \bar{D}_1 \rightarrow \bar{D}_2 \rightarrow \bar{D}_3 \rightarrow \bar{D}_4 \rightarrow \bar{D}_5$ (Endless setting) · With pull-down resistor and Schmitt inverter built in internally, chattering can be rejected only by adding external resistor and capacitor. · Internal logic operates at switch input rise.
DOWN	19		· Input pin for setting number-of-selections program in downward direction $\bar{D}_1 \leftarrow \bar{D}_2 \leftarrow \bar{D}_3 \leftarrow \bar{D}_4 \leftarrow \bar{D}_5$ (Endless setting) · Other functions are the same as for input pin for setting number-of-selections program in upward direction.
$\overline{INH}$	20		· Pin for inhibiting operation of unrecorded section sense unit and recorded section sense unit · Input low level causes inhibit mode. · Normally, inhibit mode is released only during music selection. · It is possible to freely program number of selections even at inhibit mode. · With built-in Schmitt inverter and FF which memorizes inhibit mode

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AUDIO-USE MOS IC CASE OUTLINES

● All of Sanyo audio-use MOS IC case outlines are illustrated below.

● All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.

● No marking is indicated.

Case Outline—[3003A] unit: mm

SANYO: DIP14

Case Outline—[3010A] unit: mm

SANYO: DIP22

Case Outline—[3006B] unit: mm

SANYO: DIP16

Case Outline—[3012A] unit: mm

SANYO: DIP28

Case Outline—[3007A] unit: mm

SANYO: DIP18

Case Outline—[3014A] unit: mm

SANYO: DIP42

Case Outline—[3008A] unit: mm

SANYO: DIP20

Case Outline—[3020A] unit: mm

SANYO: SEP16

Case Outline—[3021B] unit: mm

SANYO: DIP20S11m

Case Outline—[3036B] unit: mm

SANYO: MFP20

Case Outline—[3025B] unit: mm

SANYO: DIP42S

Case Outline—[3044B] unit: mm

SANYO: QIP80A

Case Outline—[3026B] unit: mm

SANYO: QIP64B

Case Outline—[3045B] unit: mm

SANYO : MFP24

Case Outline—[3029A] unit: mm

SANYO: DIP28S

Case Outline—[3047A] unit: mm

SANYO: DIP30S

Case Outline—[3035A] unit: mm

SANYO : MFP 16

Case Outline—[3052A] unit: mm

SANYO: QIP48A

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T-90-20

Case Outline—[3057] unit: mm

SANYO: QIP64A

Case Outline—[3084] unit: mm

SANYO: DIP-24Slim

Case Outline—[3063] unit: mm

SANYO: DIP28SN

Case Outline—[3118] unit: mm

SANYO: QIP48B

Case Outline—[3067] unit: mm

SANYO: DIP24S

Case Outline—[3073A] unit: mm

SANYO:MFP30

Case Outline—[3074] unit: mm

SANYO:QIP80B