512K x 16Bit x 2Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Dual banks operation
- MRS cycle with address key programs
  - CAS Latency (2 & 3)
  - Burst Length (1, 2, 4, 8 & full page)
  - Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 32ms refresh period (2K cycle)

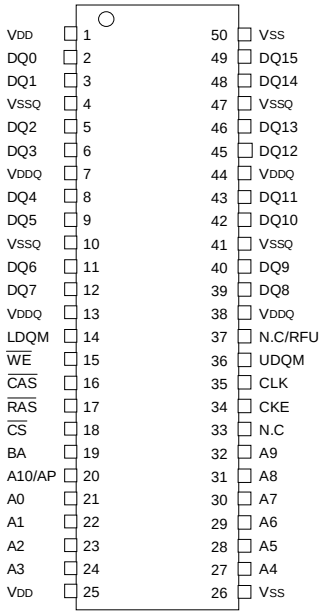
GENERAL DESCRIPTION

The M12L16161A is 16,777,216 bits synchronous high data rate Dynamic RAM organized as 2 x 524,288 words by 16 bits, fabricated with high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

Part NO.	MAX Freq.	Interface	Package
M12L16161A-4.3T	233MHz	LVTTL	50 TSOP(II)
M12L16161A-5T	200MHz		
M12L16161A-5.5T	183MHz		
M12L16161A-6T	166MHz		
M12L16161A-7T	143MHz		
M12L16161A-8T	125MHz		

PIN CONFIGURATION (TOP VIEW)



50PIN TSOP(II)
(400mil x 825mil)
(0.8 mm PIN PITCH)

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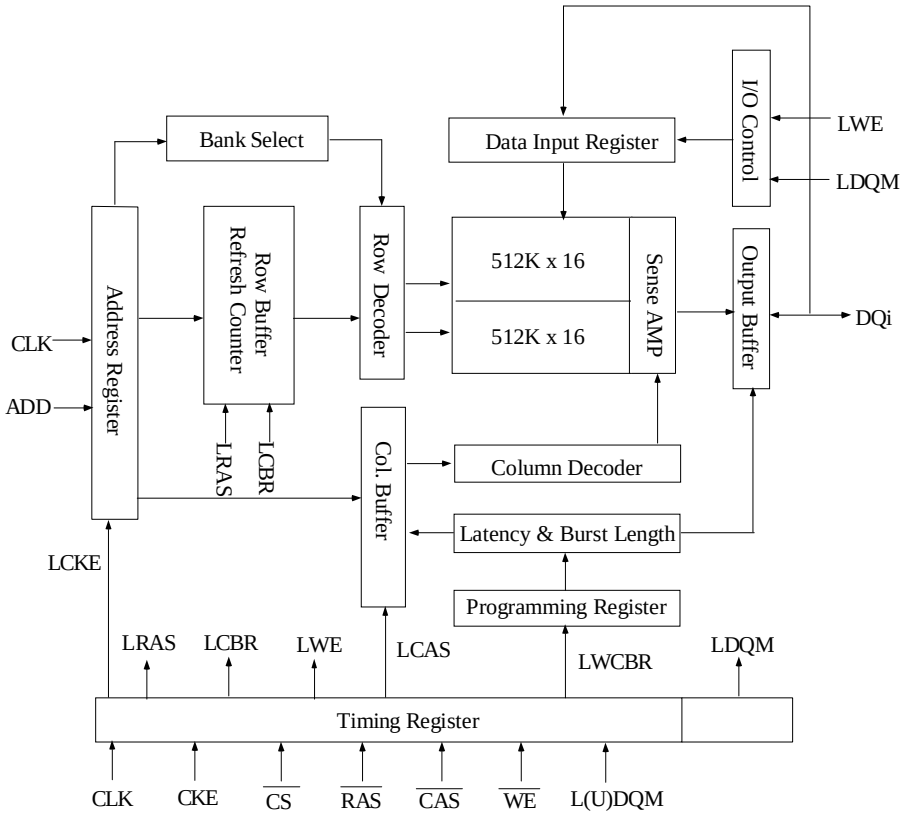
FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM.
CKE	*Clock Enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A10/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, column address : CA0 ~ CA7
BA	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	*Data Input / Output Mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when L(U)DQM active.
$DQ_{0 \sim 15}$	*Data Input / Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

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V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No Connection/ Reserved for Future Use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD},V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ + 150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	MA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to VSS = 0V, TA=0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD},V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} =-2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1.V_{IH} (max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2.V_{IL} (min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3.Any input 0V≤ V_{IN} ≤ V_{DD}+ 0.3V, all other pins are not under test = 0V.
4.Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DD}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 25 °C , f = 1MHz)

Pin	Symbol	Min	Max	Unit
CLOCK	C_{CLK}	2.5	4.0	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, LDQM, UDQM	C_{IN}	2.5	5.0	pF
ADDRESS	C_{ADD}	2.5	5.0	pF
DQ0 ~DQ15	C_{OUT}	4.0	6.5	pF

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DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70 °C V_{IH}(min)/V_{IL}(max)=2.0V/0.8V)

Parameter	Symbol	Test Condition	CAS Latency	Version -4.3	-5	-5.5	-6	-7	-8	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length = 1 $t_{RC} \geq t_{RC}$ (min), $t_{CC} \geq t_{CC}$ (min), I_{OL}= 0mA		250	230	210	190	160	140	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} =15ns		2						mA	
	I_{CC2PS}	CKE ≤ V_{IL}(max), CLK ≤ V_{IL}(max), t_{CC} = ∞		2							
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} =15ns Input signals are changed one time during 30ns		30						mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		2						mA	
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} =15ns		10						mA	
	I_{CC3PS}	CKE ≤ V_{IL}(max), CLK ≤ V_{IL}(max), t_{CC} = ∞		10							
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		40						mA	
	I_{CC3NS}	CKE ≥ V_{IH} (min), CLK ≤ V_{IL}(max), t_{CC}=∞ Input signals are stable		10						mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL}= 0Ma, Page Burst All Band Activated, t_{CCD} = t_{CCD} (min)	3	270	250	230	210	180	160	mA	1
			2	270	250	230	210	180	160		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		270	250	230	210	180	160	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		1						mA	

Note: 1.Measured with outputs open. Addresses are changed only one time during t_{CC}(min).

2.Refresh period is 32ms. Addresses are changed only one time during t_{CC}(min).

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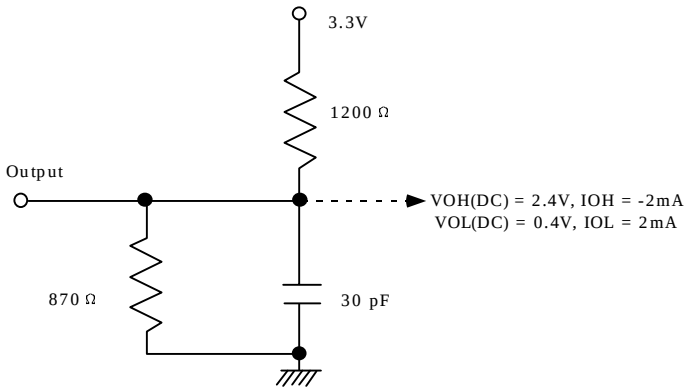
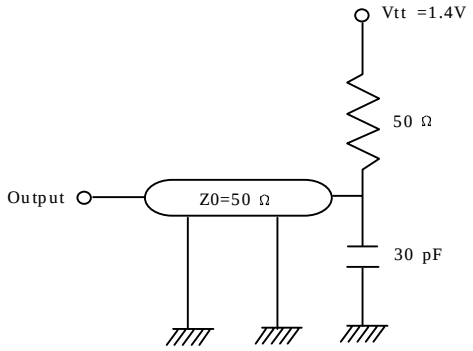
AC OPERATING TEST CONDITIONS (V_{DD}=3.3V ± 0.3V,T_A= 0 to 70°C)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig.2	



(Fig.1) DC Output Load circuit



(Fig.2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version						Unit	Note
		-4.3	-5	-5.5	-6	-7	-8		
Row active to row active delay	t_{RRD}(min)	8.6	10	11	12	14	16	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD}(min)	12.9	15	16	16	16	20	ns	1
Row precharge time	t_{RP}(min)	12.9	15	16	18	20	20	ns	1
Row active time	t_{RAS}(min)	34.4	40	40	42	42	48	ns	1
	t_{RAS}(max)	100						us	
Row cycle time	t_{RC}(min)	47.3	55	60	60	63	68	ns	1
Last data in to new col. Address delay	t_{CDL}(min)	1						CLK	2
Last data in to row precharge	t_{RDL}(min)	1						CLK	2
Last data in to burst stop	t_{BDL}(min)	1						CLK	2
Col. Address to col. Address delay	t_{CCD}(min)	1						CLK	3
Number of valid output data	CAS latency=3	1						ea	4
	CAS latency=2	1							

Note: 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
4. Minimum delay is required to complete write.
4. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
The earliest a precharge command can be issued after a Read command without the loss of data is CL+BL-2 clocks.

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AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-4.3		-5		-5.5		-6		-7		-8		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS Latency =3	t_{CC}	4.3	1000	5	1000	5.5	1000	6	1000	7	1000	8	1000	ns	1
	CAS Latency =2		6		7		7.5		8		8.6		10			
CLK to valid output delay	CAS Latency =3	t_{SAC}	-	4	-	4.5	-	5	-	5.5	-	6	-	6	ns	1
	CAS Latency =2		-	5	-	5	-	6	-	6	-	6	-	7		
Output data hold time		t_{OH}	2		2		2.5		2.5		2.5		2.5		ns	2
CLK high pulse width		t_{CH}	1.7		2		2		2		2.5		3		ns	3
CLK low pulse width		t_{CL}	1.7		2		2		2		2.5		3		ns	3
Input setup time		t_{SS}	1.7		2		2		2		2		2.5		ns	3
Input hold time		t_{SH}	1		1		1		1		1		1		ns	3
CLK to output in Low-Z		t_{SLZ}	1		1		1		1		1		1		ns	2
CLK to output in Hi-Z	CAS Latency =3	t_{SHZ}	-	4	-	4.5	-	5	-	5.5	-	6	-	6	ns	
	CAS latency =2		-	5	-	5	-	6	-	6	-	6	-	7		

*All AC parameters are measured from half to half.

Note: 1.Parameters depend on programmed CAS latency.

2.If clock rising time is longer than 1ns,(tr/2-0.5)ns should be added to the parameter.

3.Assumed input rise and fall time (tr & tf)=1ns.

If tr & tf is longer than 1ns, transient time compensation should be considered, i.e., [(tr+ tf)/2-1]ns should be added to the parameter.

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FREQUENCY vs. AC PARAMENTER RELATIONAHIP TABLE

M12L16161A-4.3T

(Unit: number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		47.3ns	34.3ns	12.9ns	8.6ns	12.9ns	4.3ns	4.3ns	4.3ns
233MHz(4.3ns)	3	11	8	3	2	3	1	1	1
200MHz(5.0ns)	3	10	7	3	2	3	1	1	1
183MHz(5.5ns)	3	10	7	3	2	3	1	1	1
166MHz(6.0ns)	3	9	6	3	2	3	1	1	1
143MHz(7.0ns)	2	7	5	2	2	2	1	1	1

M12L16161A-5T

(Unit: number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		55ns	40ns	15ns	10ns	15ns	5ns	5ns	5ns
200MHz(5.0ns)	3	11	8	3	2	3	1	1	1
183MHz(5.5ns)	3	10	8	3	2	3	1	1	1
166MHz(6.0ns)	3	10	7	3	2	3	1	1	1
143MHz(7.0ns)	2	9	6	3	2	3	1	1	1
125MHz(8.0ns)	2	7	5	2	2	2	1	1	1
111MHz(9.0ns)	2	7	5	2	2	2	1	1	1

M12L16161A-5.5T

(Unit: number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		60ns	40ns	16ns	11ns	16ns	5.5ns	5.5ns	5.5ns
183MHz(5.5ns)	3	11	8	3	2	3	1	1	1
166MHz(6.0ns)	3	10	7	3	2	3	1	1	1
143MHz(7.0ns)	2	9	6	3	2	3	1	1	1
125MHz(8.0ns)	2	8	5	2	2	2	1	1	1
111MHz(9.0ns)	2	7	5	2	2	2	1	1	1

M12L16161A-6T

(Unit: number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		60ns	42ns	18ns	12ns	16ns	6ns	6ns	6ns
166MHz(6.0ns)	3	10	7	3	2	3	1	1	1
143MHz(7.0ns)	3	9	6	3	2	3	1	1	1
125MHz(8.0ns)	2	9	6	3	2	2	1	1	1
111MHz(9.0ns)	2	7	5	2	2	2	1	1	1
100MHz(10.0ns)	2	7	5	2	2	2	1	1	1

M12L16161A-7T

(Unit: number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		62ns	42ns	20ns	14ns	16ns	7ns	7ns	7ns
143MHz(7.0ns)	3	9	6	3	2	3	1	1	1
125MHz(8.0ns)	3	9	6	3	2	2	1	1	1
111MHz(9.0ns)	2	8	5	3	2	2	1	1	1
100MHz(10.0ns)	2	7	5	2	2	2	1	1	1
83MHz(12.0ns)	2	6	4	2	2	2	1	1	1

M12L16161A-8T

(Unit: number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		68ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz(8.0ns)	3	9	6	3	2	3	1	1	1
111MHz(9.0ns)	3	9	6	3	2	3	1	1	1
100MHz(10.0ns)	2	7	5	2	2	2	1	1	1
83MHz(12.0ns)	2	6	4	2	2	2	1	1	1
75MHz(13.0ns)	2	6	4	2	2	2	1	1	1

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Mode Register

11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	1								JEDEC Standard Test Set (refresh counter test)
11	10	9	8	7	6	5	4	3	2	1	0	
x	x	1	0	0	LTMODE			WT	BL			Burst Read and Single Write (for Write Through Cache)
11	10	9	8	7	6	5	4	3	2	1	0	
			1	0								Use in future
11	10	9	8	7	6	5	4	3	2	1	0	
x	x	x	1	1	v	v	v	v	v	v	v	Vender Specific
11	10	9	8	7	6	5	4	3	2	1	0	v =Valid
0	0	0	0	0	LTMODE			WT	BL			Mode Register Set x =Don't care

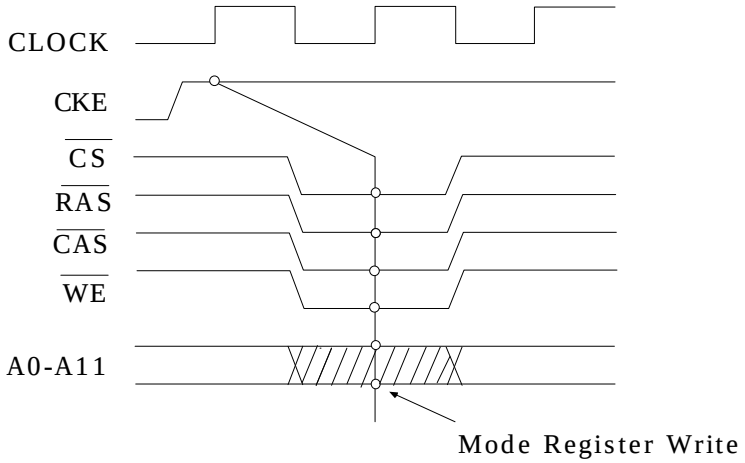
	Bit2-0	WT=0	WT=1
Burst length	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	Full page	R

Wrap type	0	Sequential
	1	Interleave

	Bits6-4	$\overline{\text{CAS}}$ Latency
Latency mode	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
	111	R

Remark R : Reserved

Mode Register Write Timing



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Burst Length and Sequence

(Burst of Two)

Starting Address (column address A0 binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0,1	0,1
1	1,0	1,0

(Burst of Four)

Starting Address (column address A1-A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
00	0,1,2,3	0,1,2,3
01	1,2,3,0	1,0,3,2
10	2,3,0,1	2,3,0,1
11	3,0,1,2	3,2,1,0

(Burst of Eight)

Starting Address (column address A2-A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
000	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
001	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
010	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
011	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
100	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
101	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
110	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
111	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0

Full page burst is an extension of the above tables of Sequential Addressing, with the length being 256 for 1Mx16 divice.

POWER UP SEQUENCE

1.Apply power and start clock, attempt to maintain CKE= “H”, L(U)DQM = “H” and the other pin are NOP condition at the inputs.

2.Maintain stable power, stable clock and NOP input condition for a minimum of 200us.

3.Issue precharge commands for all banks of the devices.

4.Issue 2 or more auto-refresh commands.

5.Issue mode register set command to initialize the mode register.

Cf.)Sequence of 4 & 5 is regardless of the order.

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SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA	A10/AP	A9~A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
				L									3
	Self Refresh	Entry											
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4,5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4,5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	4
	Both Banks									X	H		4
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
			H		L	H	H	H					

(V= Valid, X= Don't Care, H= Logic High , L = Logic Low)

Note:1 OP Code: Operation Code

A0~ A10/AP, BA: Program keys.(@MRS)

2. MRS can be issued only at both banks precharge state.

A new command can be issued after 2 clock cycle of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".
Auto / self refresh can be issued only at both banks precharge state.

4. BA: Bank select address.

If "Low": at read, write, row active and precharge, bank A is selected.
If "High": at read, write, row active and precharge, bank B is selected.
If A10/AP is "High" at row precharge, BA ignored and both banks are selected.

5.During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read /write command can be issued after the end of burst.

New row active of the associated bank can be issued at t_{RP} after the end of burst.

6.Burst stop command is valid at every burst length.

7.DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes
Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

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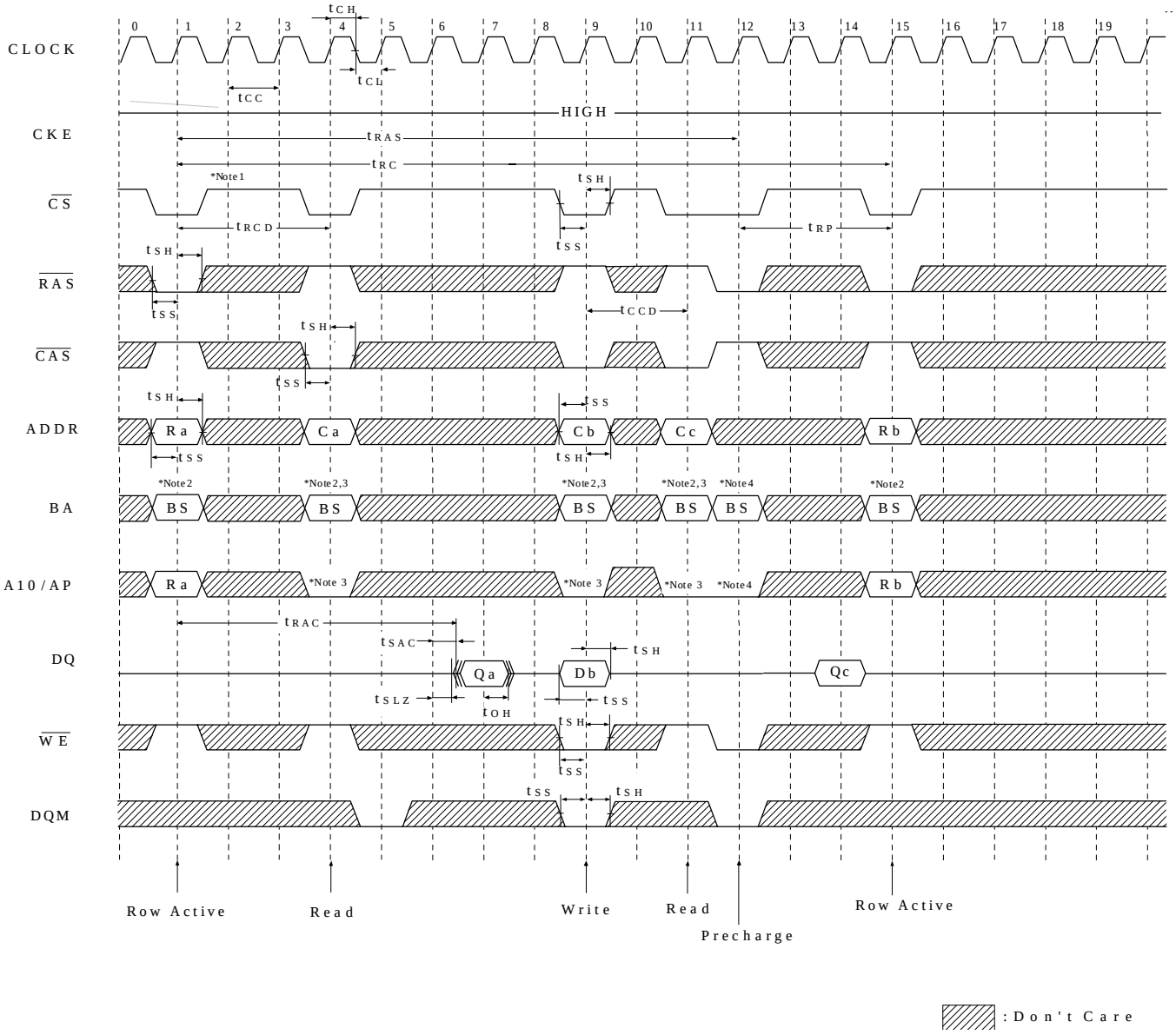
Single Bit Read-Write-Read Cycle (Same Page) @CAS Latency=3, Burst Length=1



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***Note:** 1. All inputs expect CKE & DQM can be don't care when $\overline{CS}$ is high at the CLK high going edge.

2. Bank active & read/write are controlled by BA.

BA	Active & Read/Write
0	Bank A
1	Bank B

3.Enable and disable auto precharge function are controlled by A10/AP in read/write command.

A10/AP	BA	Operation
0	0	Disable auto precharge, leave bank A active at end of burst.
	1	Disable auto precharge, leave bank B active at end of burst.
1	0	Enable auto precharge, precharge bank A at end of burst.
	1	Enable auto precharge, precharge bank B at end of burst.

4.A10/AP and BA control bank precharge when precharge command is asserted.

A10/AP	BA	precharge
0	0	Bank A
0	1	Bank B
1	X	Both Banks

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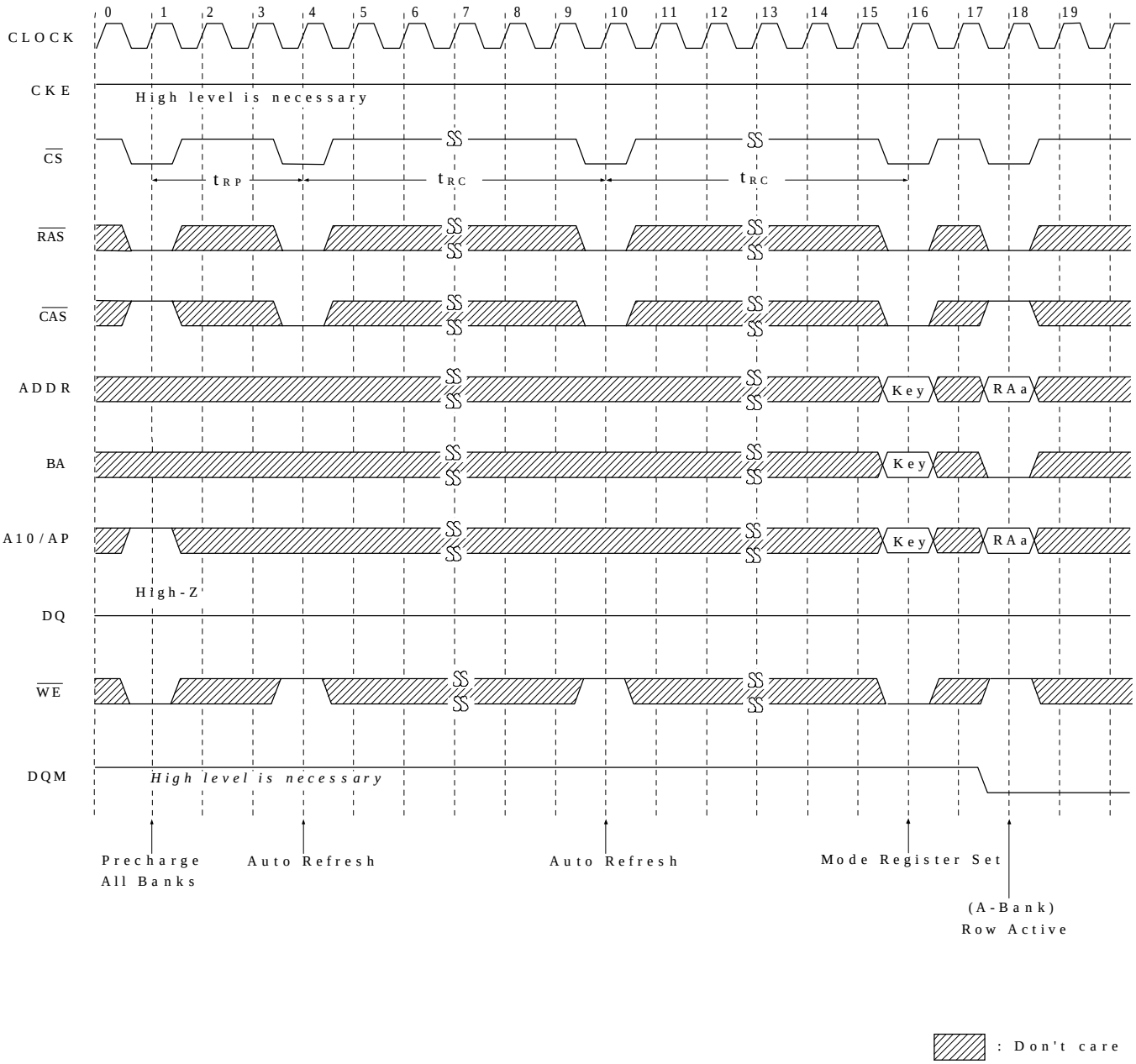
Power Up Sequence



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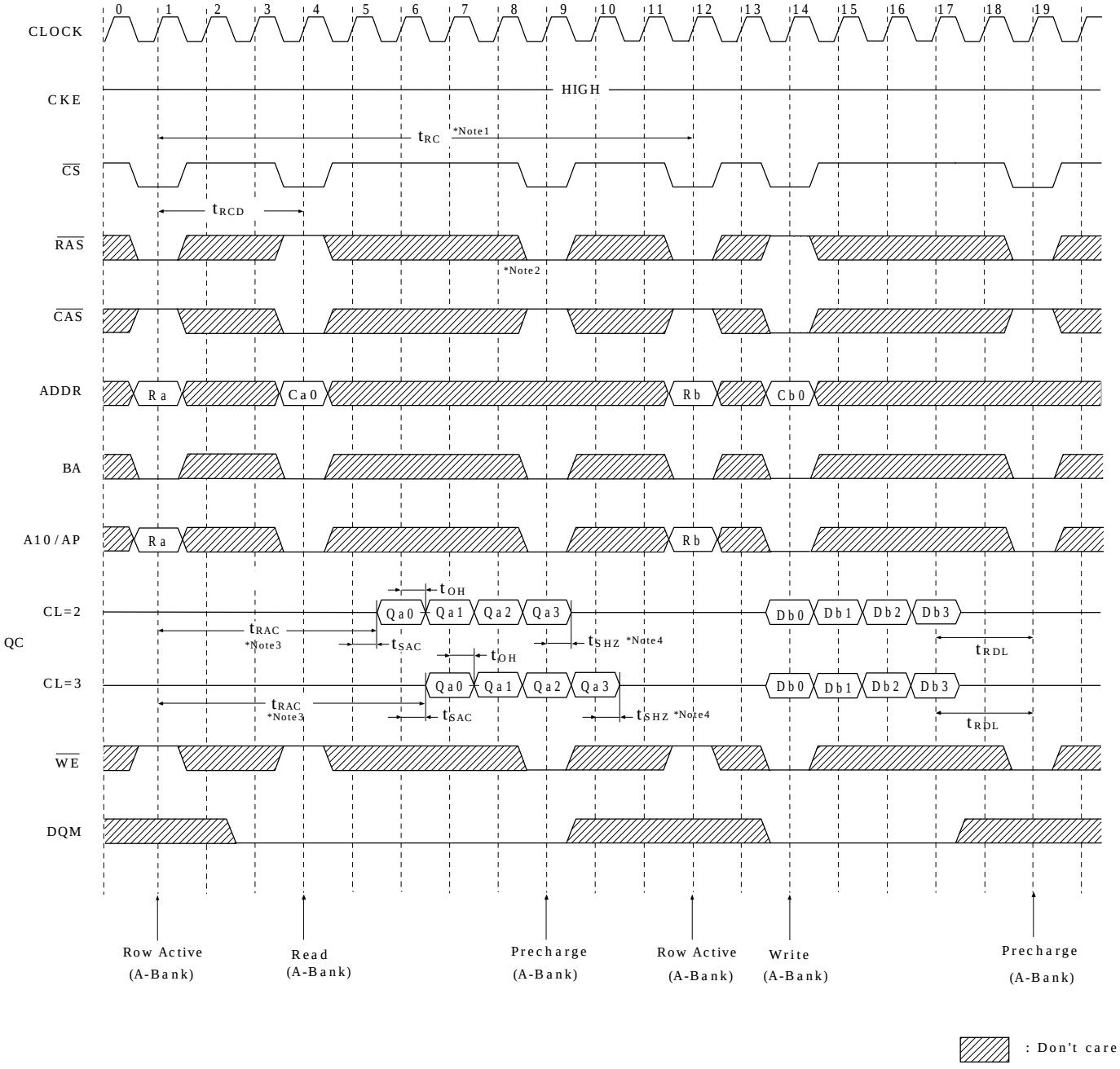
Read & Write Cycle at Same Bank @Burst Length = 4



***Note:** 1.Minimum row cycle times is required to complete internal DRAM operation.

2.Row precharge can interrupt burst on any cycle. [CAS Latency-1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{SHZ}) after the clock.

3.Access time from Row active command. tcc*(t_{RCD} +CAS latency-1)+t_{SAC}

4.Ouput will be Hi-Z after the end of burst.(1,2,4,8 bit burst)

Burst can't end in Full Page Mode.

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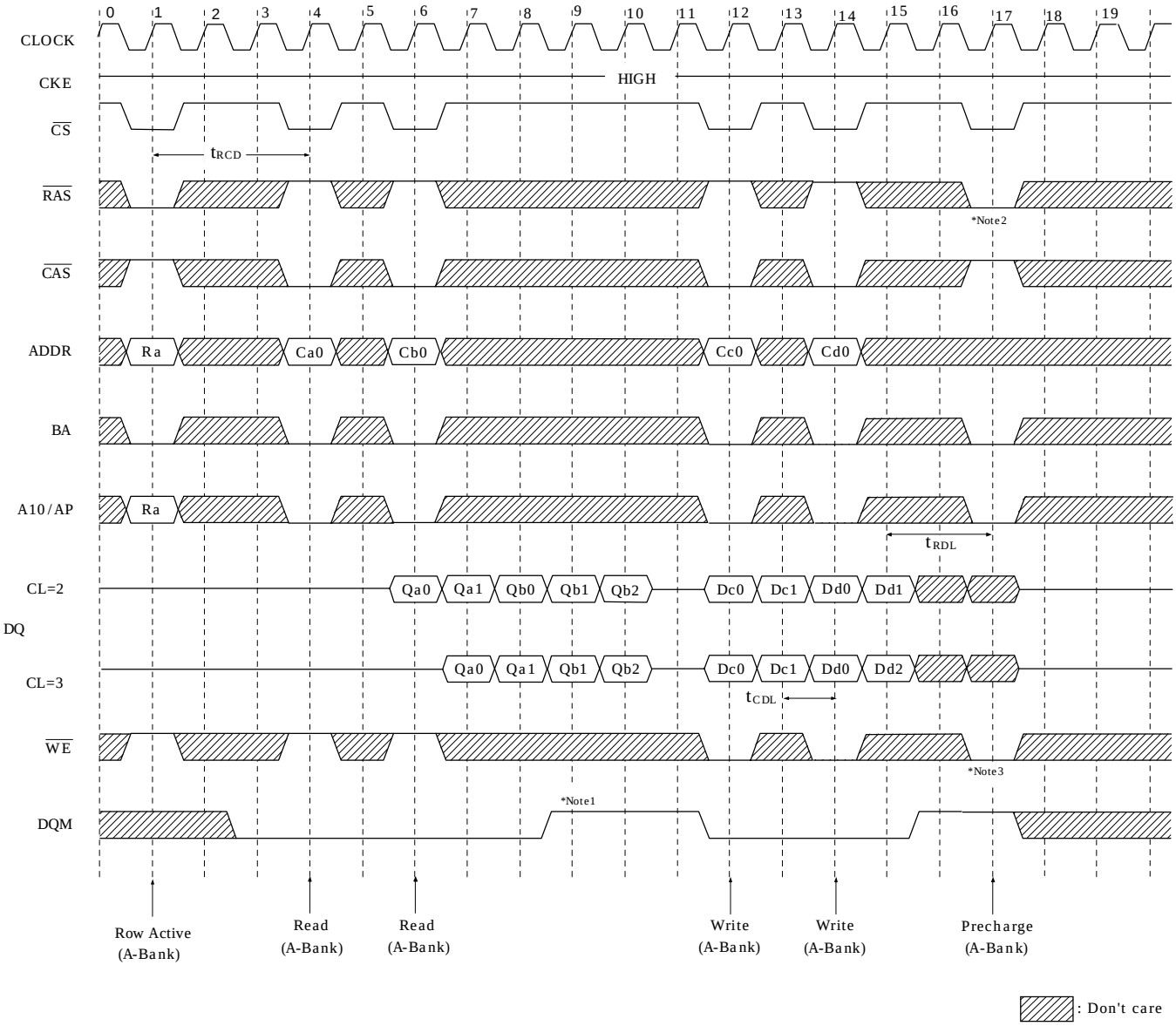
Page Read & Write Cycle at Same Bank @ Burst Length=4



***Note :** 1.To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.

2.Row precharge will interrupt writing. Last data input, t_{RDL} before Row precharge, will be written.

3.DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

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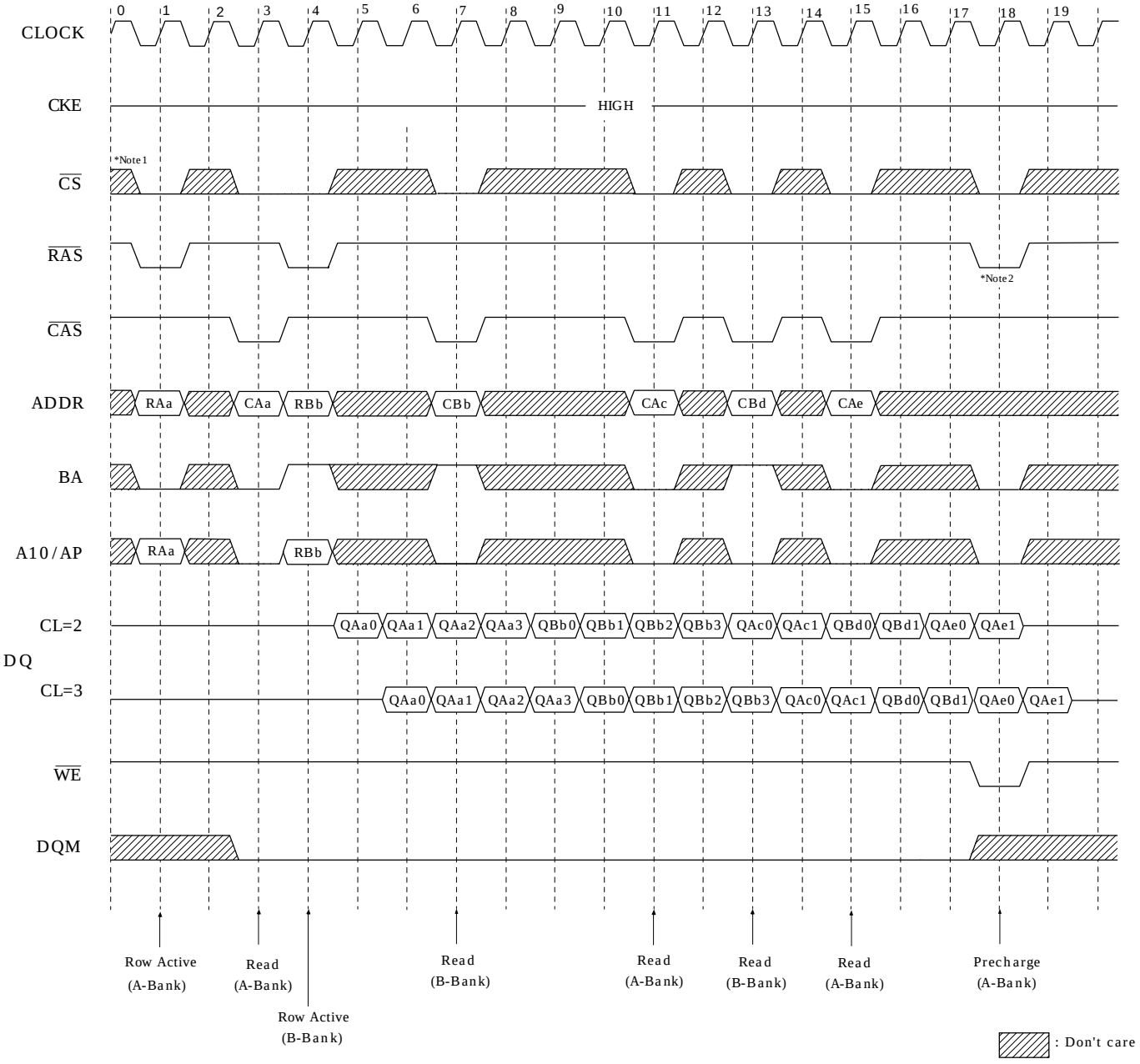
Page Read Cycle at Different Bank @ Burst Length=4



*Note: 1. $\overline{CS}$ can be don't cared when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the clock high going dege.

2.To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

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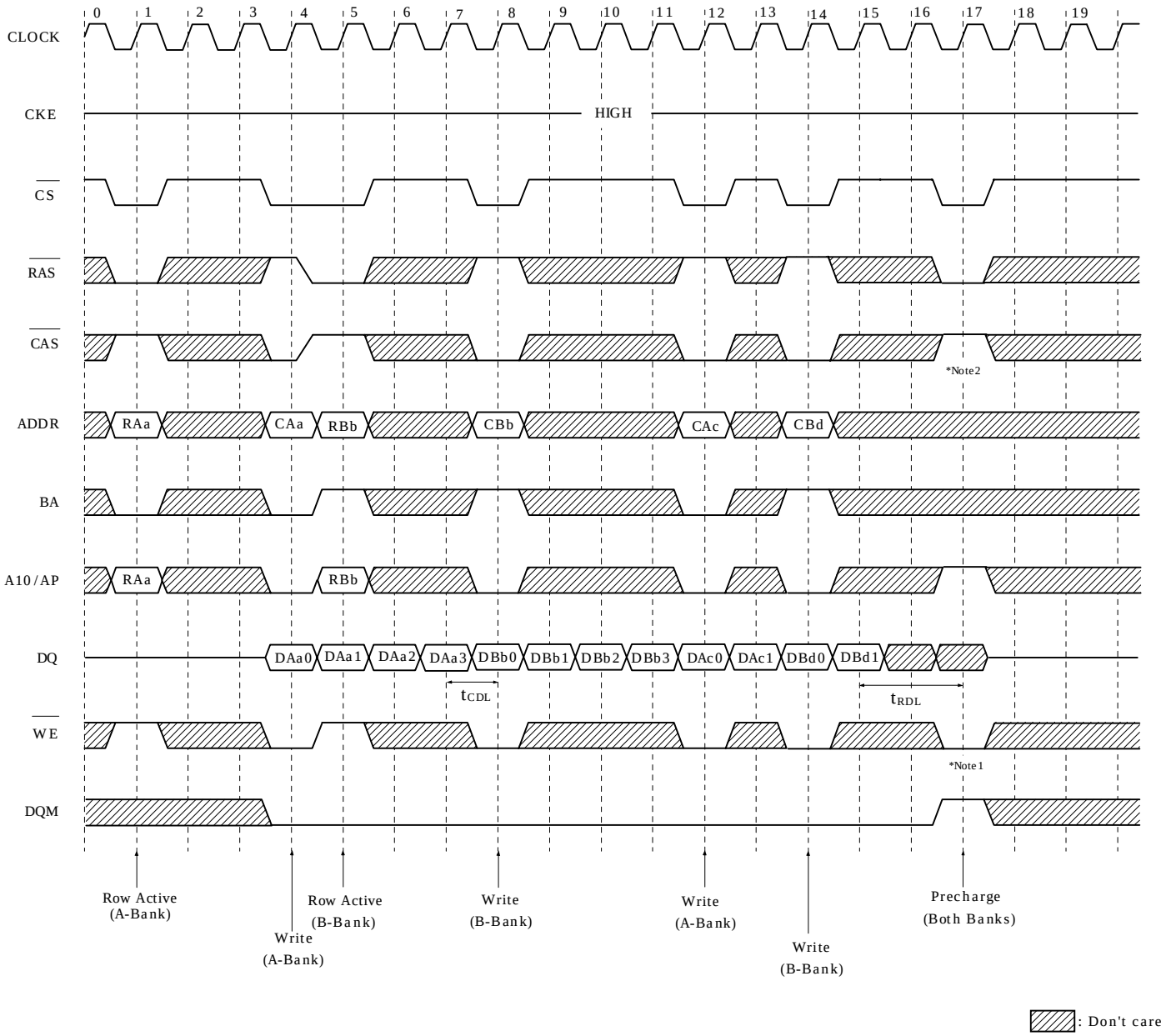
Page Write Cycle at Different Bank @Burst Length = 4



*Note: 1.To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.

2.To interrupt burst write by row precharge, both the write and the precharge banks must be the same.

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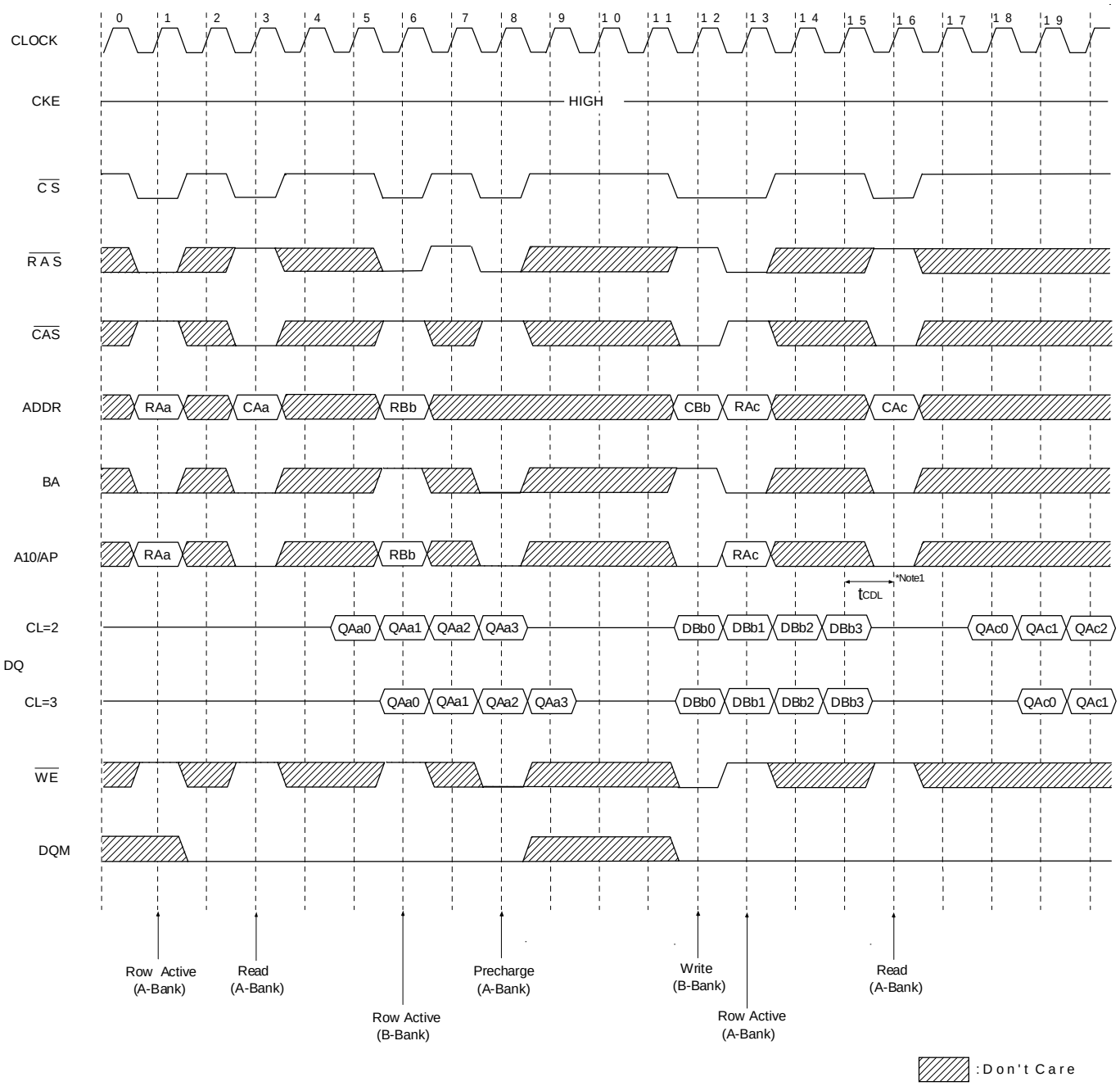
Read & Write Cycle at Different Bank @ Burst Length = 4



*Note: 1.t_{CDL} should be met to complete write.

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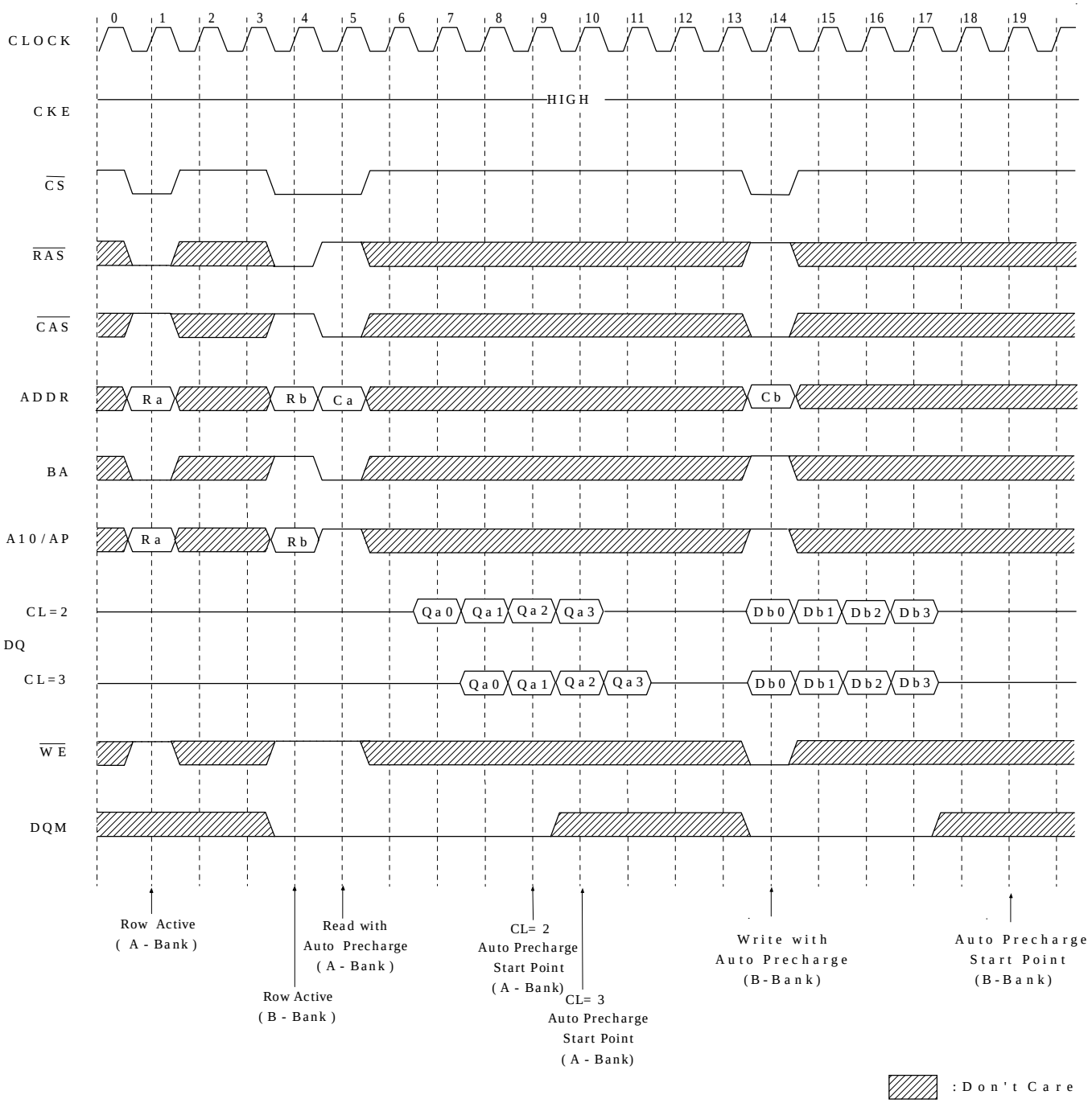
Read & Write Cycle with auto Precharge @ Burst Length =4



*Note: 1.t_{CDL} Should be controlled to meet minimum t_{RAS} before internal precharge start

(In the case of Burst Length=1 & 2 and BRSW mode)

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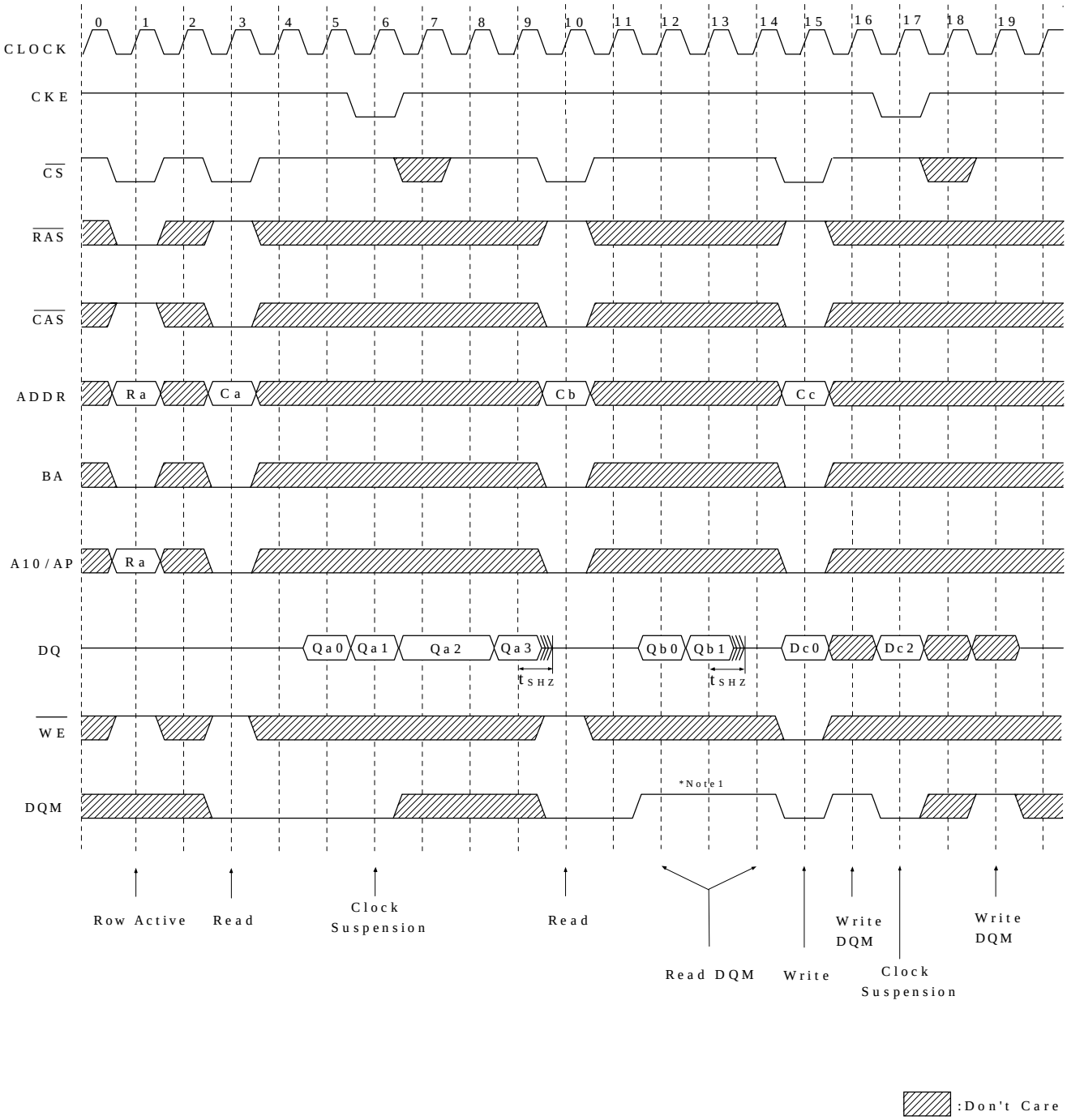
Clock Suspension & DQM Operation Cycle @CAS Latency=2, Burst Length=4



*Note:1.DQM is needed to prevent bus contention.

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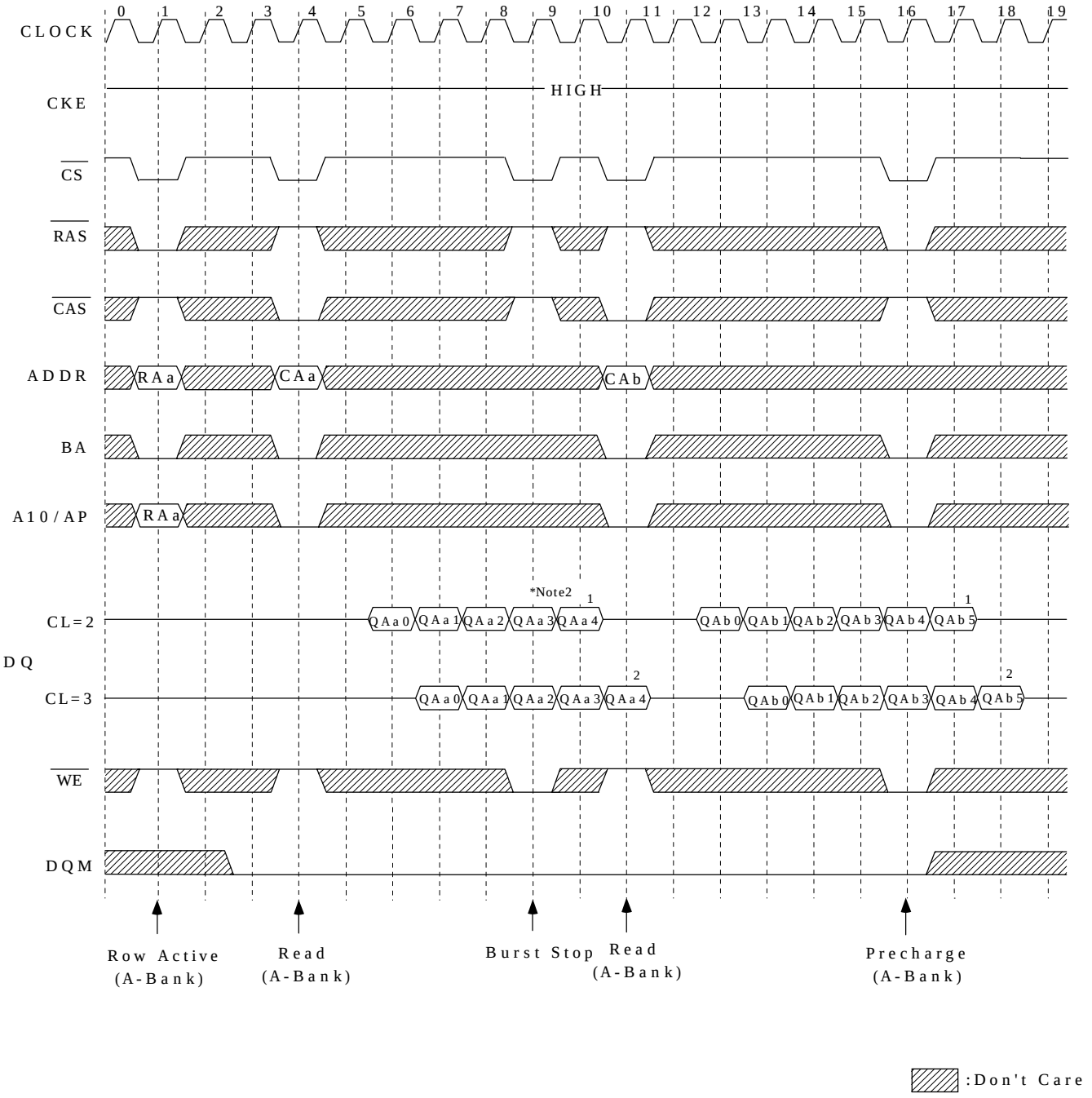
Read Interrupted by Precharge Command & Read Burst Stop Cycle @Burst Length =Full page



***Note:** 1.Burst can't end in full page mode, so auto precharge can't issue.

2.About the valid DQs after burst stop, it is same as the case of $\overline{RAS}$ interrupt.

Both cases are illustrated above timing diagram. See the label 1,2 on them.

But at burst write, burst stop and $\overline{RAS}$ interrupt should be compared carefully.

Refer the timing diagram of "Full page write burst stop cycle".

3.Burst stop is valid at every burst length.

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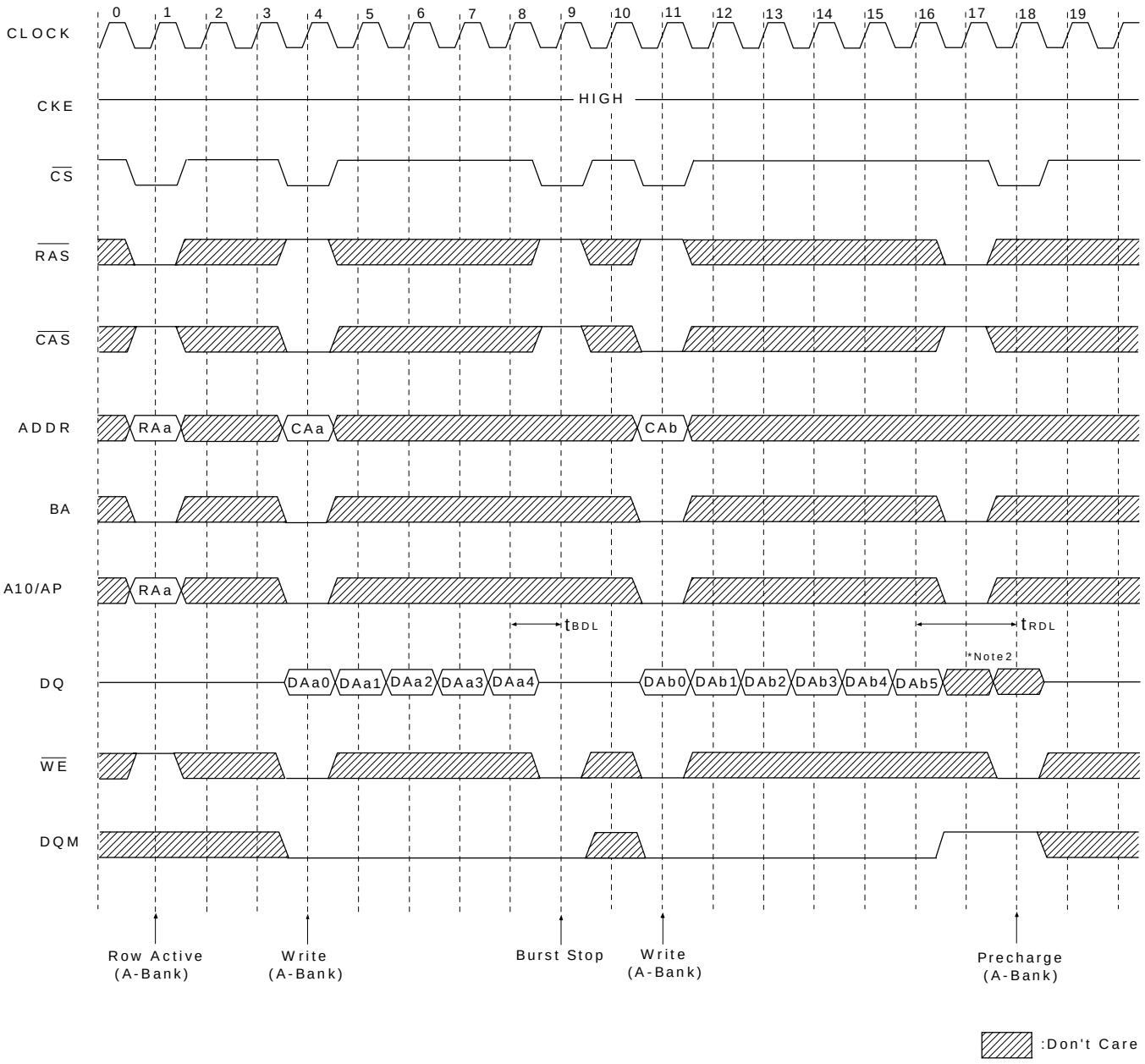
Write Interrupted by Precharge Command & Write Burst stop Cycle @ Burst Length =Full page



***Note:** 1. Burst can't end in full page mode, so auto precharge can't issue.

2.Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}.

DQM at write interrupted by precharge command is needed to prevent invalid write.

Input data after Row precharge cycle will be masked internally.

3.Burst stop is valid at every burst length.

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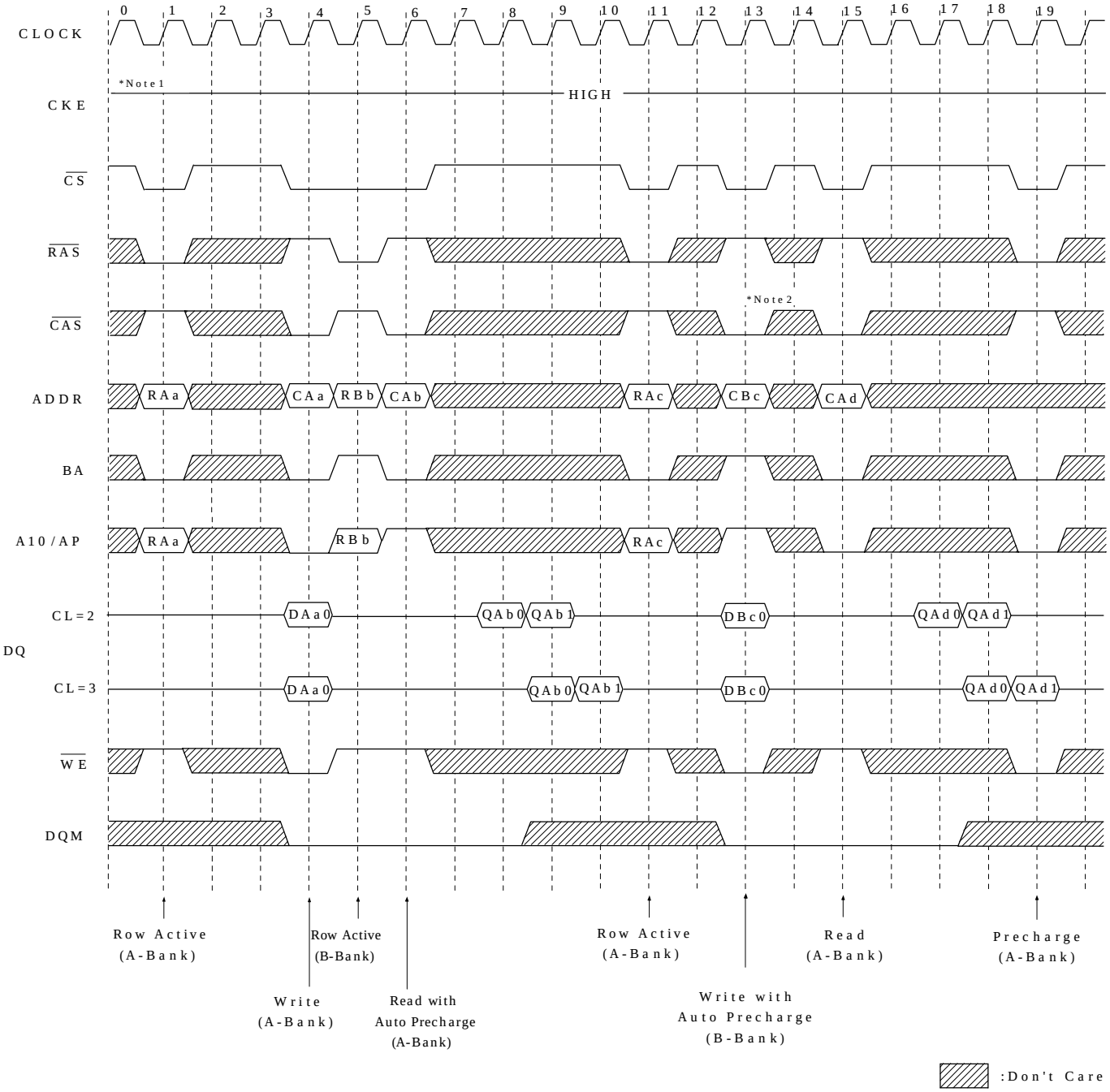
Burst Read Single bit Write Cycle @Burst Length=2



*Note:1.BRSW modes is enabled by setting A9 "High" at MRS(Mode Register Set).

At the BRSW Mode, the burst length at write is fixed to "1" regardless of programmed burst length.

2.When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated.

Auto precharge is executed at the next cycle of burst-end, so in the case of BRSW write command, the precharge command will be issued after two clock cycles.

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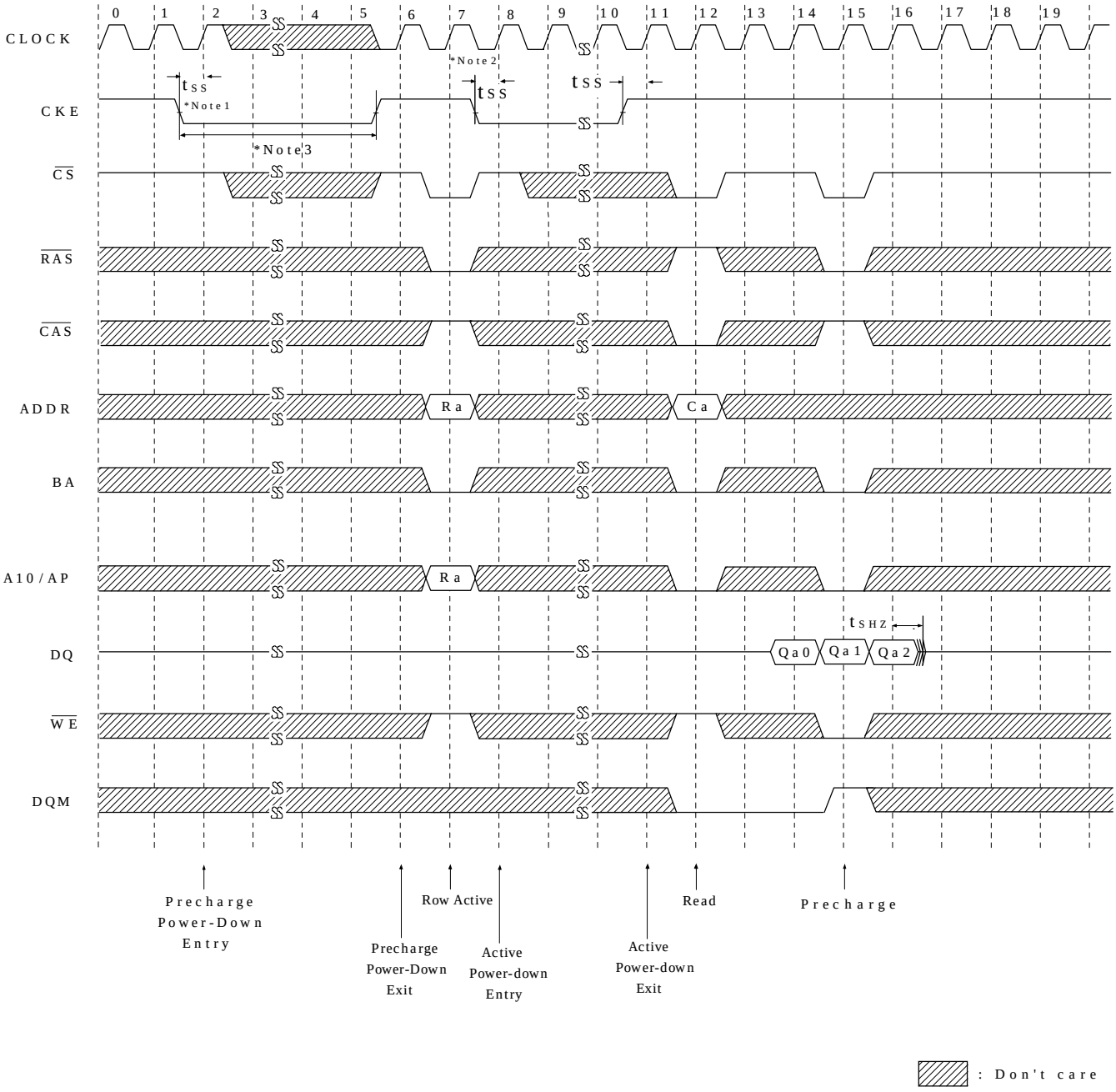
Active/Precharge Power Down Mode @CAS Latency=2, Burst Length=4



***Note :** 1.Both banks should be in idle state prior to entering precharge power down mode.

2.CKE should be set high at least 1CLK+tss prior to Row active command.

3.Can not violate minimum refresh specification. (32ms)

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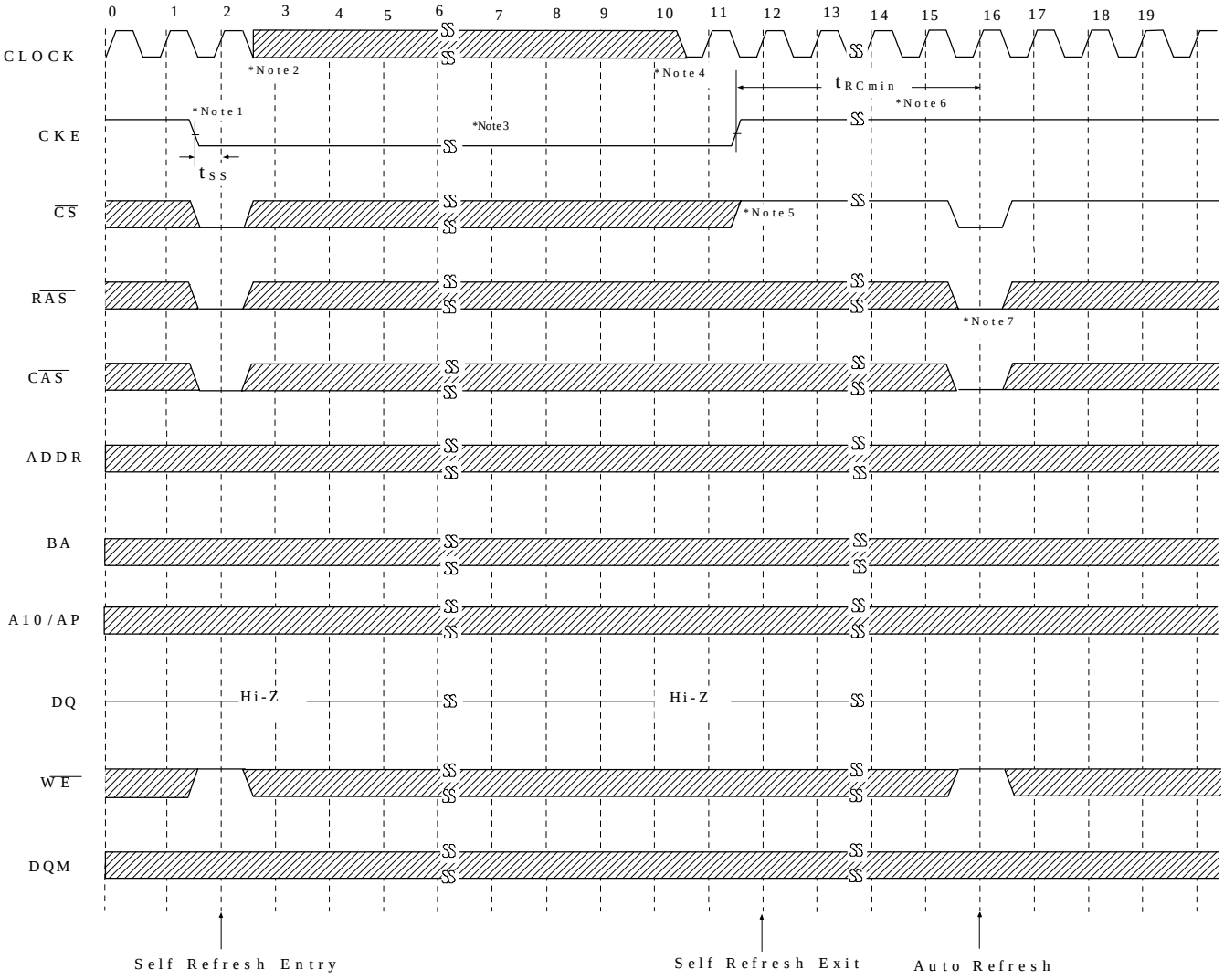
Self Refresh Entry & Exit Cycle



***Note: TO ENTER SELF REFRESH MODE**

1. $\overline{CS}$, $\overline{RAS}$ & $\overline{CAS}$ with CKE should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "Low".

cf.) Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning CKE high.
5. $\overline{CS}$ Starts from high.
6. Minimum t_{RC} is required after CKE going high to complete self refresh exit.
7. 2K cycle of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

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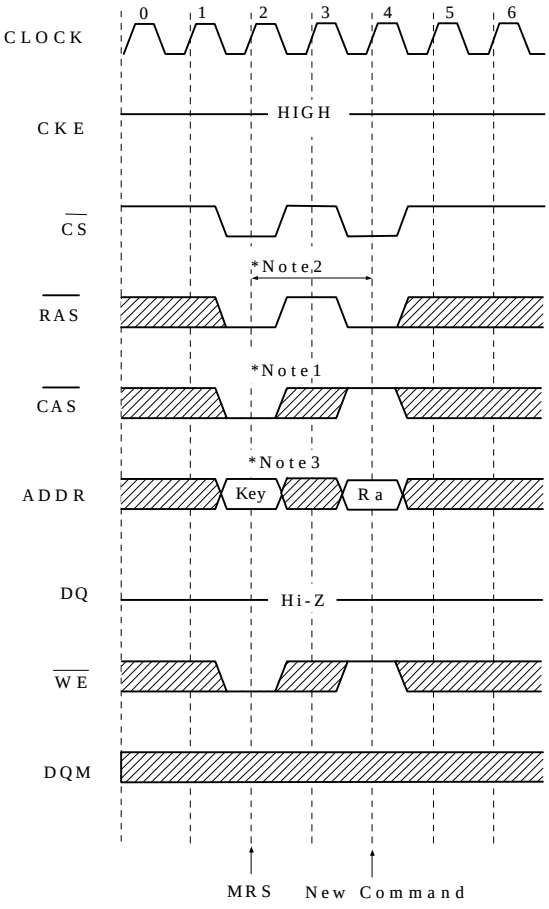
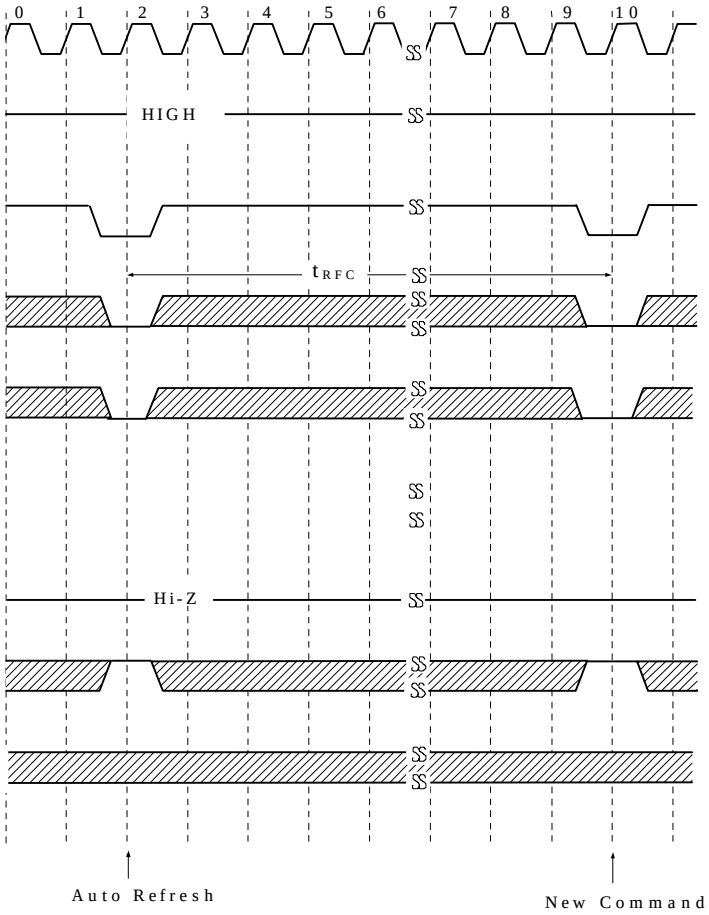
Mode Register Set Cycle



Auto Refresh Cycle



:Don't Care

*Both banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

MODE REGISTER SET CYCLE

*Note: 1. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ & $\overline{WE}$ activation at the same clock cycle with address key will set internal mode register.

2.Minimum 2 clock cycles should be met before new $\overline{RAS}$ activation.

3.Please refer to Mode Register Set table.

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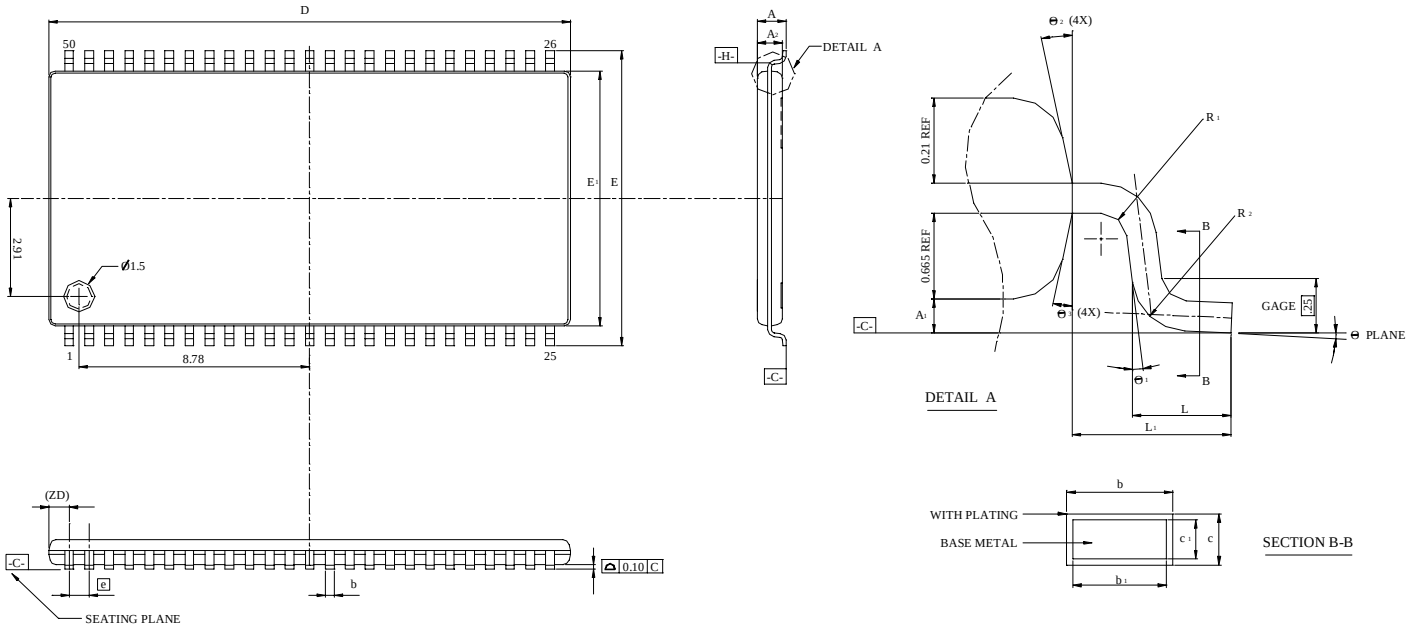
PACKAGE DIMENSIONS
50-LEAD TSOP(II) SDRAM(400mil)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.20	-	-	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	-	0.45	0.012	-	0.018
b1	0.30	0.35	0.40	0.012	0.014	0.016
c	0.12	-	0.21	0.005	-	0.008
c1	0.10	0.127	0.16	0.004	0.005	0.006
D	20.82	20.95	21.08	0.820	0.825	0.830
ZD		0.875 REF			0.034 REF	
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.394	0.400	0.405
L	0.40	0.50	0.60	0.016	0.020	0.024
L1		0.80 REF			0.031 REF	
		0.80 BSC			0.031 BSC	
R1	0.12	-	-	0.005	-	
R2	0.12	-	0.25	0.005	-	0.010
θ	0	-	8	0	-	8
θ 1	0	-	-	0	-	-
θ 2	10	15	20	10	15	20
θ 3	10	15	20	10	15	20

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