TOP100-4

TOPSwitch® Family

Three-terminal Off-line PWM Switch

Product Highlights

Low Cost Replacement for Discrete Switchers

- 20 to 50 fewer components - cuts cost, increases reliability
- Source-connected tab and Controlled MOSFET turn-on reduce EMI and EMI filter costs
- Allows for a 50% smaller and lighter solution
- Cost competitive with linears above 5 W

Up to 90% Efficiency in Flyback Topology

- Built-in start-up and current limit reduce DC losses
- Low capacitance 350 V MOSFET cuts AC losses
- CMOS controller/gate driver consumes only 6 mW
- 70% maximum duty cycle minimizes conduction losses

Simplifies Design - Reduces Time to Market

- Supported by many reference designs
- Integrated PWM Controller and 350 V MOSFET in a industry standard three pin TO-220 package
- Only one external capacitor needed for compensation, bypass and start-up/auto-restart functions

System Level Fault Protection Features

- Auto-restart and cycle by cycle current limiting functions handle both primary and secondary faults
- On-chip latching thermal shutdown protects the entire system against overload

Highly Versatile

- Implements Buck, Boost, Flyback or Forward topology
- Easily interfaces with both opto and primary feedback
- Supports continuous or discontinuous mode of operation
- Specified for operation down to 16 V DC input

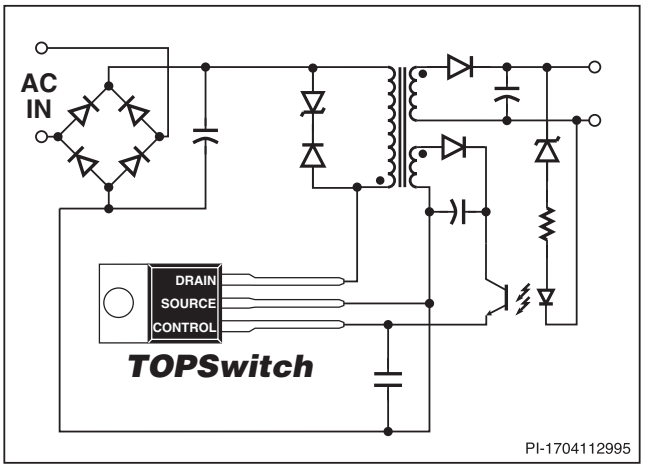


Figure 1. Typical Application.

TOPSwitch SELECTION GUIDE			
ORDER PART NUMBER	OUTPUT POWER RANGE		
	FLYBACK		PFC/ BOOST
	100/110 V VAC	48 V DC	100/110 VAC
TOP100YN*	0-20 W	0-6.8 W	0-30 W
TOP101YN*	15-35 W	6-12 W	25-50 W
TOP102YN*	20-45 W	8.5-17 W	35-70 W
TOP103YN*	25-55 W	11-22 W	45-90 W
TOP104YN*	30-60 W	12-25 W	55-110 W

* Package Outline: Y03A

Description

The *TOPSwitch* family implements, with only three pins, all functions necessary for an off-line switched mode control system: high voltage N-channel power MOSFET with controlled turn-on gate driver, voltage mode PWM controller with integrated 100 kHz oscillator, high voltage start-up bias circuit, bandgap derived reference, bias shunt regulator/error amplifier for loop compensation and fault protection circuitry. Compared to discrete MOSFET and controller or self oscillating (RCC) switching converter solutions, a *TOPSwitch* integrated circuit can reduce total cost, component count, size, weight and at the same time increase efficiency and system reliability. These devices are intended for 100/110 VAC off-line Power Supply applications in the 0 to 60 W range and power factor correction (PFC) applications in the 0 to 110 W range. They are also well suited for Telecom, Cablecom and other DC to DC converter applications in the 0-25 W range (see Design Note DN-16).

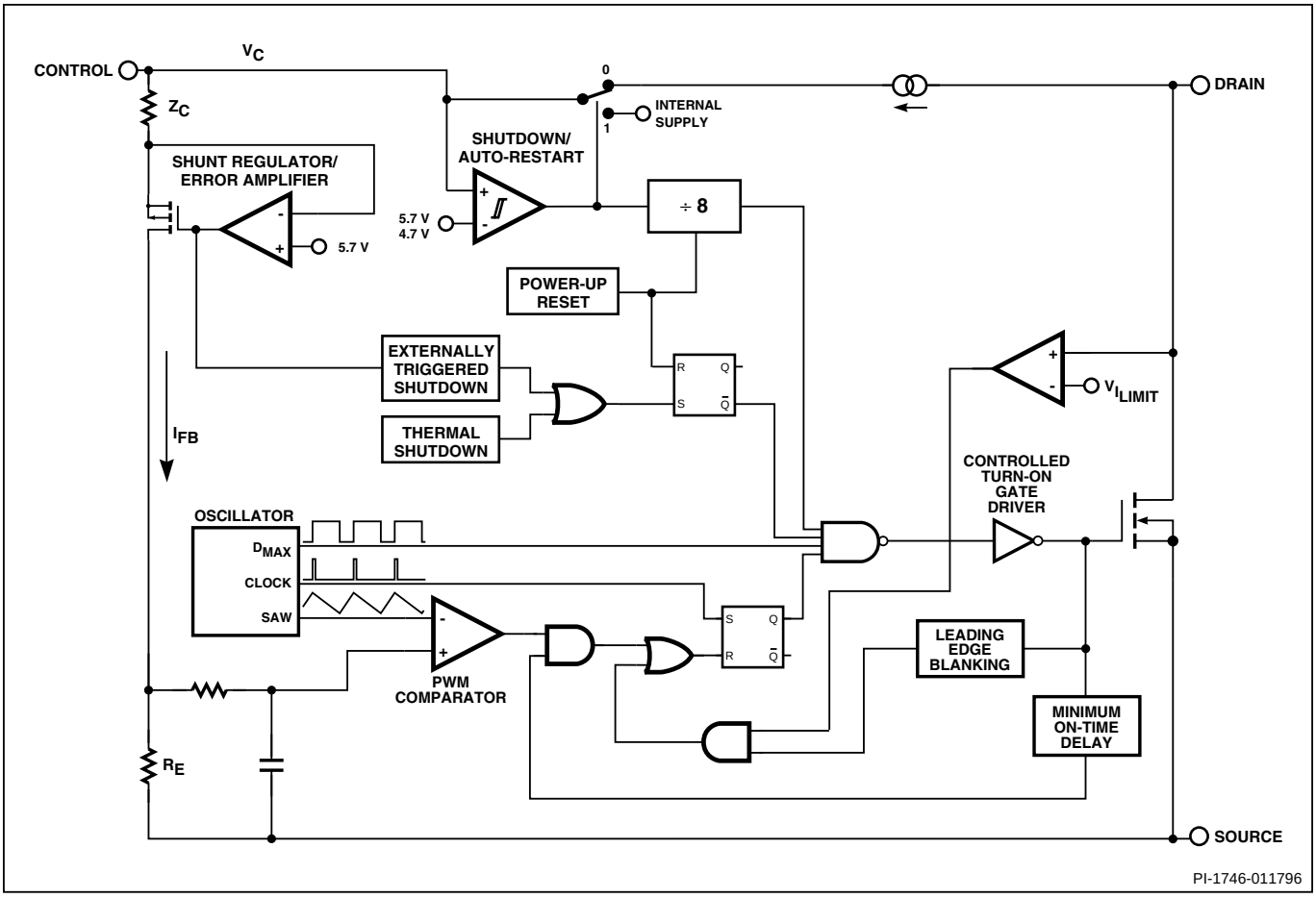


Figure 2. Functional Block Diagram.

Pin Functional Description

DRAIN Pin:
Output MOSFET drain connection. Provides internal bias current during start-up operation via an internal switched high-voltage current source. Internal current sense point.

CONTROL Pin:
Error amplifier and feedback current input pin for duty cycle control. Internal shunt regulator connection to provide internal bias current during normal operation. Trigger input for latching shutdown. It is also used as the supply bypass and auto-restart/ compensation capacitor connection point.

SOURCE Pin:
Output MOSFET source connection. Primary-side circuit common, power return, and reference point.

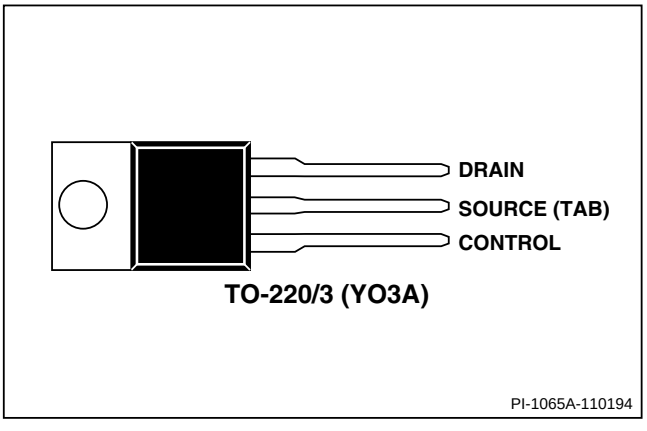


Figure 3. Pin Configuration.

TOPSwitch Family Functional Description

TOPSwitch is a self biased and protected linear control current-to-duty cycle converter with an open drain output. High efficiency is achieved through the use of CMOS and integration of the maximum number of functions possible. CMOS significantly reduces bias currents as compared to bipolar or discrete solutions. Integration eliminates external power resistors used for current sensing and/or supplying initial start-up bias current.

During normal operation, the internal output MOSFET duty cycle linearly decreases with increasing CONTROL pin current as shown in Figure 4. To implement all the required control, bias, and protection functions, the DRAIN and CONTROL pins each perform several functions as described below. Refer to Figure 2 for a block diagram and Figure 6 for timing and voltage waveforms of the *TOPSwitch* integrated circuit.

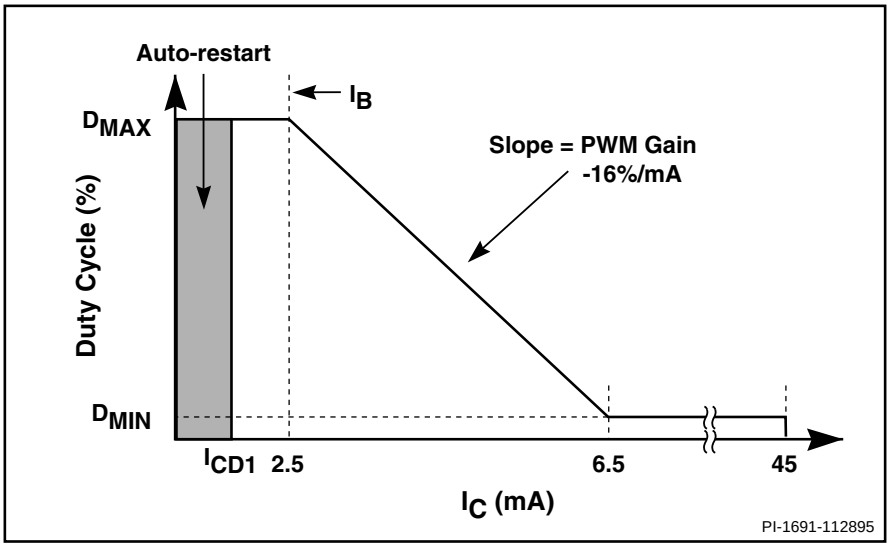


Figure 4. Relationship of Duty Cycle to CONTROL Pin Current.

Control Voltage Supply

CONTROL pin voltage V_C is the supply or bias voltage for the controller and driver circuitry. An external bypass capacitor closely connected between the CONTROL and SOURCE pins is required to supply the gate drive current. The total amount of capacitance connected to this pin (C_T) also sets the auto-restart timing as well as control loop compensation. V_C is regulated in either of two modes of operation. Hysteretic regulation is used for initial start-up and overload operation. Shunt regulation is used to separate the duty cycle error signal from the control circuit supply current. During start-up, V_C current is supplied from a high-voltage switched current source connected internally between the DRAIN and CONTROL pins. The current source provides sufficient current to supply the control circuitry as well as charge the total external capacitance (C_T).

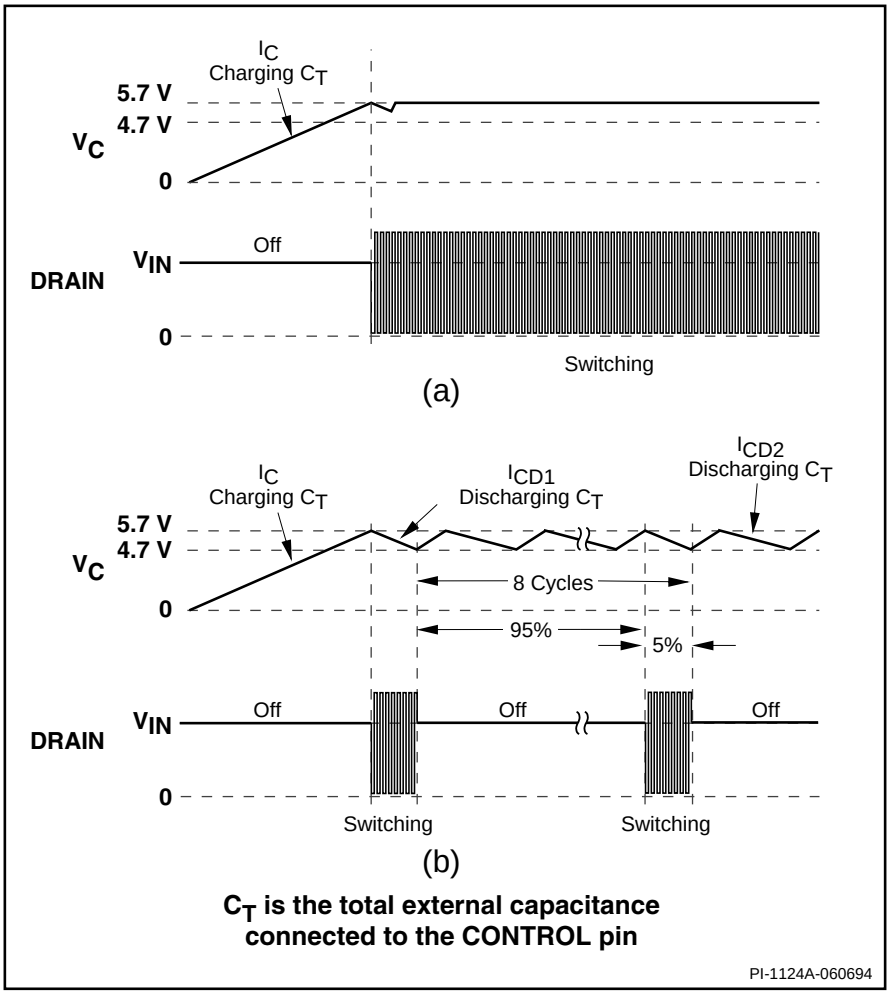


Figure 5. Start-up Waveforms for (a) Normal Operation and (b) Auto-restart.

TOPSwitch Family Functional Description (cont.)

The first time V_C reaches the upper threshold, the high-voltage current source is turned off and the PWM modulator and output transistor are activated, as shown in Figure 5(a). During normal operation (when the output voltage is regulated) feedback control current supplies the V_C supply current. The shunt regulator keeps V_C at typically 5.7 V by shunting CONTROL pin feedback current exceeding the required DC supply current through the PWM error signal sense resistor R_E. The low dynamic impedance of this pin (Z_C) sets the gain of the error amplifier when used in a primary feedback configuration. The dynamic impedance of the CONTROL pin together with the external resistance and capacitance determines the control loop compensation of the power system.

If the CONTROL pin external capacitance (C_T) should discharge to the lower threshold, then the output MOSFET is turned off and the control circuit is placed in a low-current standby mode. The high-voltage current source is turned on and charges the external capacitance again. Charging current is shown with a negative polarity and discharging current is shown with a positive polarity in Figure 6. The hysteretic auto-restart comparator keeps V_C within a window of typically 4.7 to 5.7 V by turning the high-voltage current source on and off as shown in Figure 5(b). The auto-restart circuit has a divide-by-8 counter which prevents the output MOSFET from turning on again until eight discharge-charge cycles have elapsed. The counter effectively limits *TOPSwitch* power dissipation by reducing the auto-restart duty cycle to typically 5%. Auto-restart continues to cycle until output voltage regulation is again achieved.

Bandgap Reference

All critical *TOPSwitch* internal voltages are derived from a temperature-compensated bandgap reference. This reference is also used to generate a temperature-compensated current source which is trimmed to accurately set the oscillator frequency and MOSFET gate drive current.

Oscillator

The internal oscillator linearly charges and discharges the internal capacitance between two voltage levels to create a sawtooth waveform for the pulse width modulator. The oscillator sets the pulse width modulator/current limit latch at the beginning of each cycle. The nominal frequency of 100 kHz was chosen to minimize EMI and maximize efficiency in power supply applications. Trimming of the current reference improves oscillator frequency accuracy.

Pulse Width Modulator

The pulse width modulator implements a voltage-mode control loop by driving the output MOSFET with a duty cycle inversely proportional to the current flowing into the CONTROL pin. The error signal across R_E is filtered by an RC network with a typical corner frequency of 7 kHz to reduce the effect of switching noise. The filtered error signal is compared with the internal oscillator sawtooth waveform to generate the duty cycle waveform. As the control current increases, the duty cycle decreases. A clock signal from the oscillator sets a latch which turns on the output MOSFET. The pulse width modulator resets the latch, turning off the output MOSFET. The maximum duty cycle is set by the symmetry of the internal oscillator. The modulator has a minimum ON-time to keep the current consumption of the *TOPSwitch* independent of the error signal. Note that a minimum current must be driven into the CONTROL pin before the duty cycle begins to change.

Gate Driver

The gate driver is designed to turn the output MOSFET on at a controlled rate to minimize common-mode EMI. The gate drive current is trimmed for improved accuracy.

Error Amplifier

The shunt regulator can also perform the function of an error amplifier in primary feedback applications. The shunt regulator voltage is accurately derived from the temperature compensated bandgap reference. The gain of the error amplifier is set by the CONTROL pin dynamic impedance. The CONTROL pin clamps external circuit signals to the V_C voltage level. The CONTROL pin current in excess of the supply current is separated by the shunt regulator and flows through R_E as the error signal.

Cycle-By-Cycle Current Limit

The cycle by cycle peak drain current limit circuit uses the output MOSFET ON-resistance as a sense resistor. A current limit comparator compares the output MOSFET ON-state drain-source voltage, $V_{DS(ON)}$, with a threshold voltage. High drain current causes $V_{DS(ON)}$ to exceed the threshold voltage and turns the output MOSFET off until the start of the next clock cycle. The current limit comparator threshold voltage is temperature compensated to minimize variation of the effective peak current limit due to temperature related changes in output MOSFET $R_{DS(ON)}$.

The leading edge blanking circuit inhibits the current limit comparator for a short time after the output MOSFET is turned on. The leading edge blanking time has been set so that current spikes caused by primary-side capacitances and secondary-side rectifier reverse recovery time will not cause premature termination of the switching pulse.

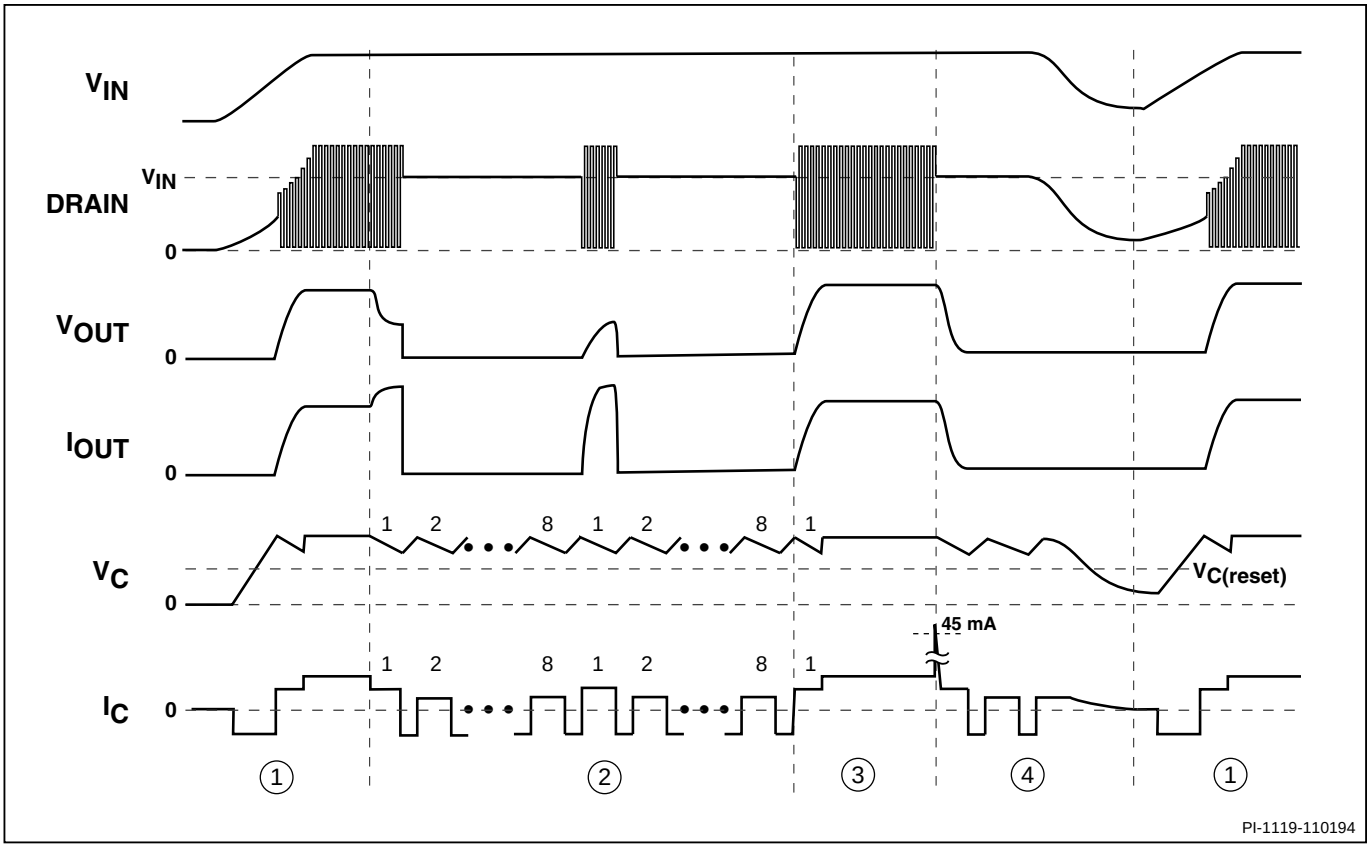


Figure 6. Typical Waveforms for (1) Normal Operation, (2) Auto-restart, (3) Latching Shutdown, and (4) Power Down Reset.

Shutdown/Auto-restart

To minimize *TOPSwitch* power dissipation, the shutdown/auto-restart circuit turns the power supply on and off at a duty cycle of typically 5% if an out of regulation condition persists. Loss of regulation interrupts the external current into the CONTROL pin. V_C regulation changes from shunt mode to the hysteretic auto-restart mode described above. When the fault condition is removed, the power supply output becomes regulated, V_C regulation returns to shunt mode, and normal operation of the power supply resumes.

Latching Shutdown

The output overvoltage protection latch is activated by a high-current pulse into the CONTROL pin. When set, the latch turns off the *TOPSwitch* output. Activating the power-up reset circuit by removing and restoring input power, or momentarily pulling the CONTROL pin below the power-up reset threshold resets the latch and allows *TOPSwitch* to resume normal power supply operation. V_C is regulated in hysteretic mode when the power supply is latched off.

Overtemperature Protection

Temperature protection is provided by a precision analog circuit that turns the output MOSFET off when the junction temperature exceeds the thermal shutdown temperature (typically 145°C). Activating the power-up reset circuit by removing and restoring input power or momentarily pulling the CONTROL pin below the power-up reset threshold resets the latch and allows *TOPSwitch* to resume normal power supply operation. V_C is regulated in hysteretic mode when the power supply is latched off.

High-voltage Bias Current Source

This current source biases *TOPSwitch* from the DRAIN pin and charges the CONTROL pin external capacitance (C_T) during start-up or hysteretic operation. Hysteretic operation occurs during auto-restart and latched shutdown. The current source is switched on and off with an effective duty cycle of approximately 35%. This duty cycle is determined by the ratio of CONTROL pin charge (I_C) and discharge currents (I_{CD1} and I_{CD2}). This current source is turned off during normal operation when the output MOSFET is switching.

General Circuit Operation

Primary Feedback Regulation
The circuit shown in Figure 7 is a simple 5 V, 5 W bias supply using the TOP100. This flyback power supply employs primary-side regulation from a transformer bias winding. This approach is best for low-cost applications requiring isolation and operation within a narrow range of load variation. Line and load regulation of ±5% or better can be achieved from 10% to 100% of rated load.

Voltage feedback is obtained from the transformer (T1) bias winding, which eliminates the need for optocoupler and secondary-referenced error amplifier. High-voltage DC is applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated high-voltage MOSFET transistor within the TOP100 (U1). The circuit operates at a switching frequency of 100 kHz, set by the internal oscillator of the TOP100. The clamp circuit implemented by VR1 and D1 limits the leading-edge voltage spike caused by transformer leakage inductance to a safe value. The 5 V power secondary winding is rectified and filtered by D2, C2, C3, and L1 to create the 5 V output voltage.

The output of the T1 bias winding is rectified and filtered by D3, R1, and C5. The voltage across C5 is regulated by U1, and is determined by the 5.7 V internal shunt regulator at the CONTROL pin of U1. When the rectified bias voltage on C5 begins to exceed the shunt regulator voltage, current will flow into the control pin. Increasing control pin current decreases the duty cycle until a stable operating point is reached. The output voltage is proportional to the bias voltage by the turns ratio of the output to bias windings. C5 is used to bypass the CONTROL pin. C5 also provides loop compensation for the power supply by shunting AC currents around the CONTROL pin dynamic impedance, and also determines the auto-restart frequency during start-up and auto-restart conditions. See DN-8 for more information regarding bias supplies.

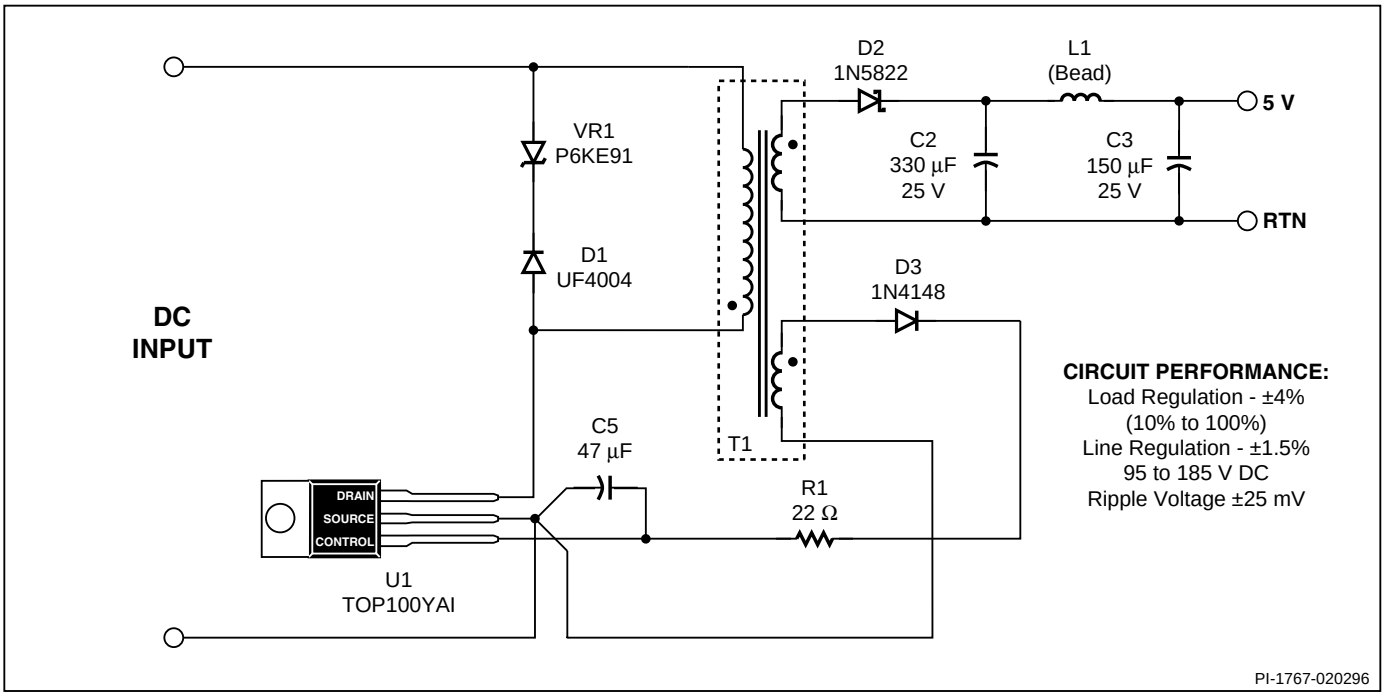


Figure 7. Schematic Diagram of a Minimum Parts Count 5 V, 5 W Bias Supply Utilizing the TOP100.

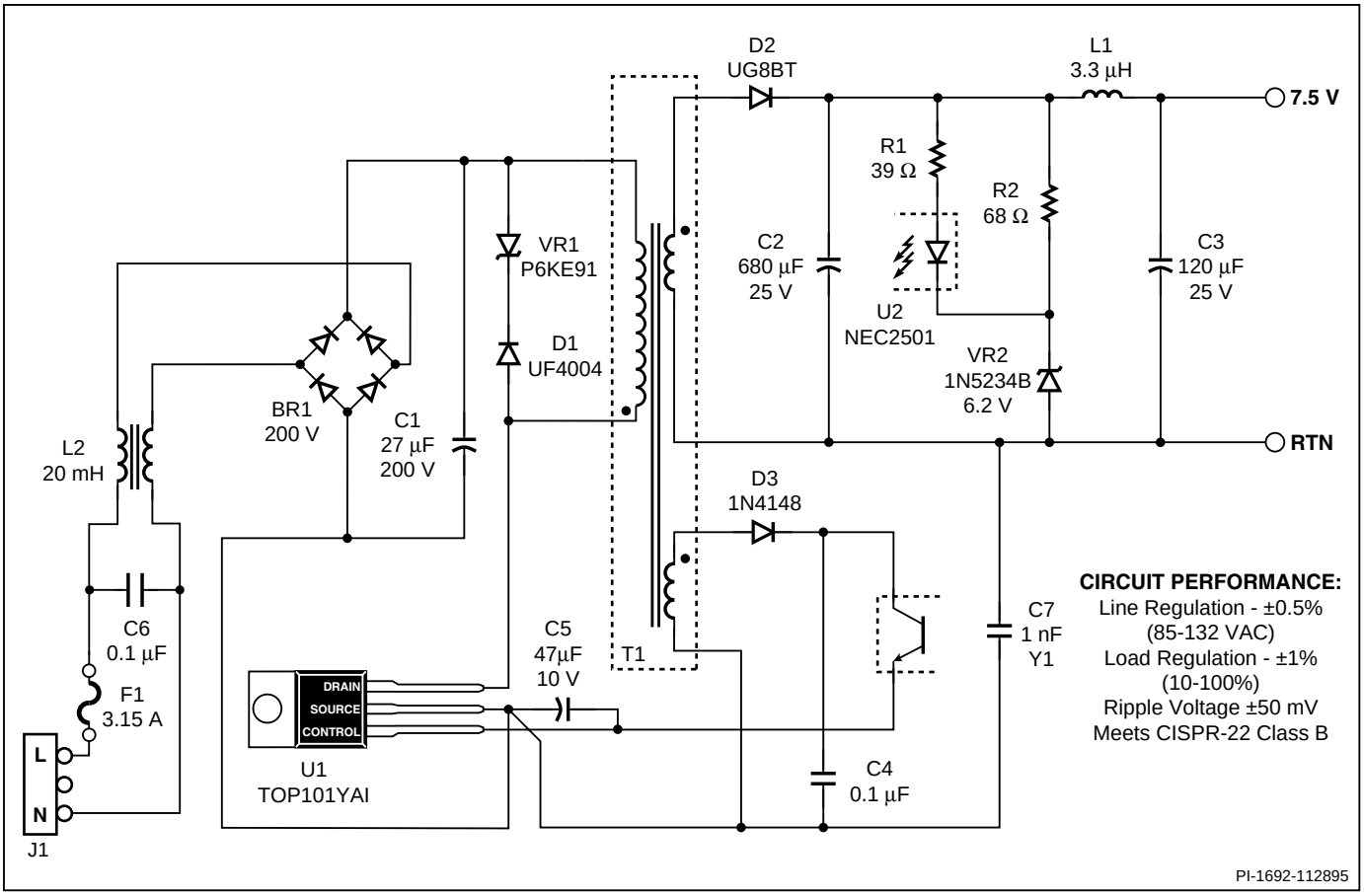


Figure 8. Schematic Diagram of a 15 W 100/110 VAC Input Power Supply Utilizing the TOP101 and Simple Optocoupler Feedback.

Simple Optocoupler Feedback

The circuit shown in Figure 8 is a 7.5 V, 15 W secondary regulated flyback power supply using the TOP101 that will operate from 85 to 132 VAC input voltage. Improved output voltage accuracy and regulation over the circuit of Figure 7 is achieved by using an optocoupler and secondary referenced Zener diode. The general operation of the power stage of this circuit is the same as that described for Figure 7.

The input voltage is rectified and filtered by BR1 and C1. L2, C6 and C7 reduce conducted emission currents. The bias winding is rectified and filtered by D3 and C4 to create a typical 11 V bias voltage. Zener diode (VR2) voltage together with the forward voltage of the LED in the optocoupler U2 determine the output voltage. R1, the optocoupler current transfer ratio, and the *TOPSwitch* control current to duty cycle transfer function set the DC control loop gain. C5 together with the control pin dynamic impedance and capacitor ESR establish a control loop pole-zero pair. C5 also determines the auto-restart frequency and filters internal gate drive switching currents. R2 and VR2 provide minimum current loading when output current is low. See DN-11 for more information regarding low-cost, 15 W power supplies.

Accurate Optocoupler Feedback

The circuit shown in Figure 9 is a highly accurate, 15 V, 30 W secondary-regulated flyback power supply that will operate from 85 to 132 VAC input voltage. A TL431 shunt regulator directly senses and accurately regulates the output voltage. The effective output voltage can be fine tuned by adjusting the resistor divider formed by R4 and R5. Other output voltages are possible by adjusting the transformer turns ratios as well as the divider ratio.

The general operation of the input and power stages of this circuit are the same as that described for Figures 7 and 8. R3 and C5 tailor frequency response. The TL431 (U3) regulates the output voltage by controlling optocoupler LED current (and *TOPSwitch* duty cycle) to maintain an average voltage of 2.5 V at the TL431 input pin. Divider R4 and R5 determine the actual output voltage. C9 rolls off the high frequency gain of the TL431 for stable operation. R1 limits optocoupler LED current and determines high frequency loop gain. For more information, refer to application note AN-14.

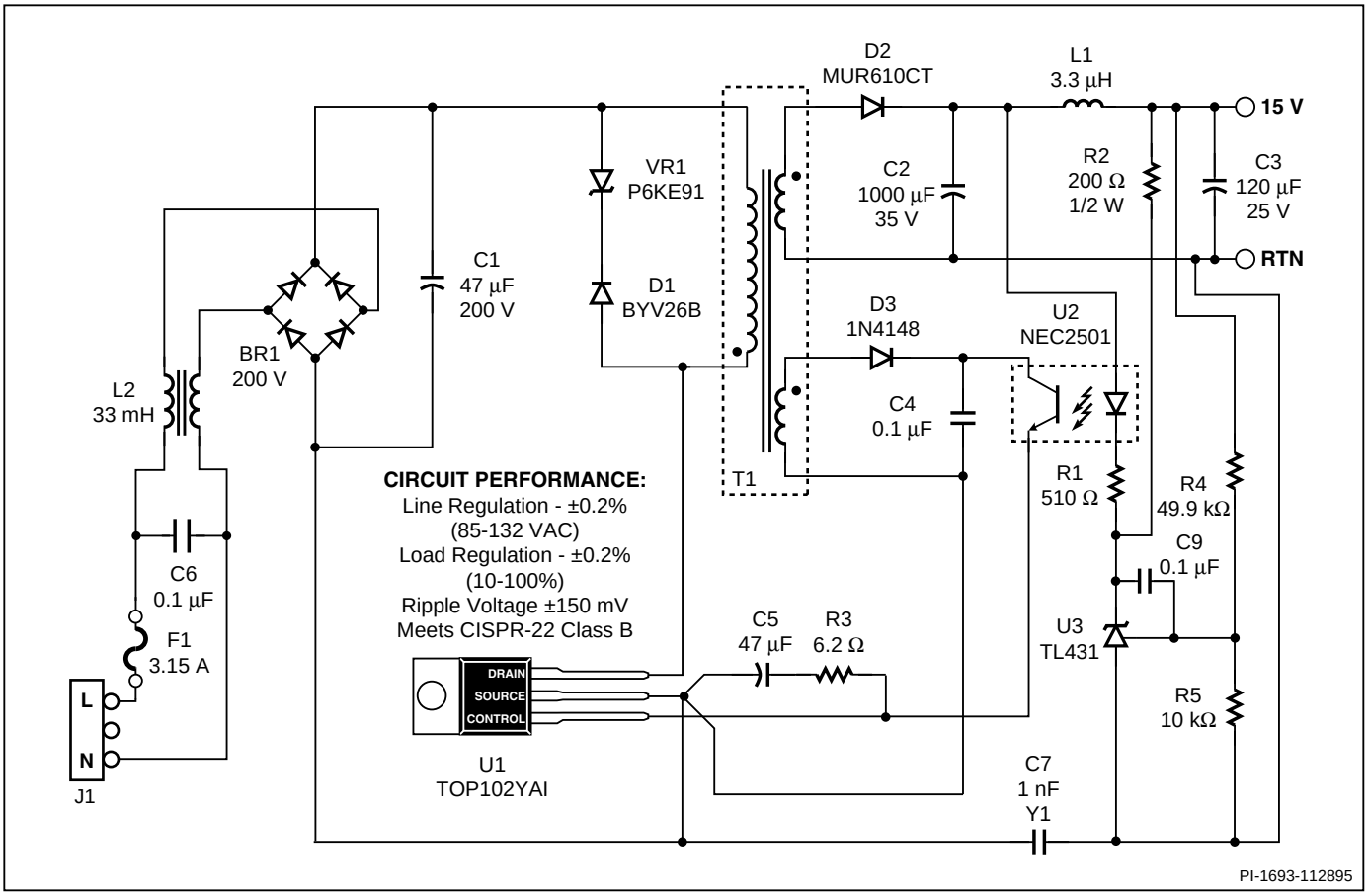


Figure 9. Schematic Diagram of a 30 W 100/110 VAC Input Power Supply Utilizing the TOP102 and Accurate Optocoupler Feedback.

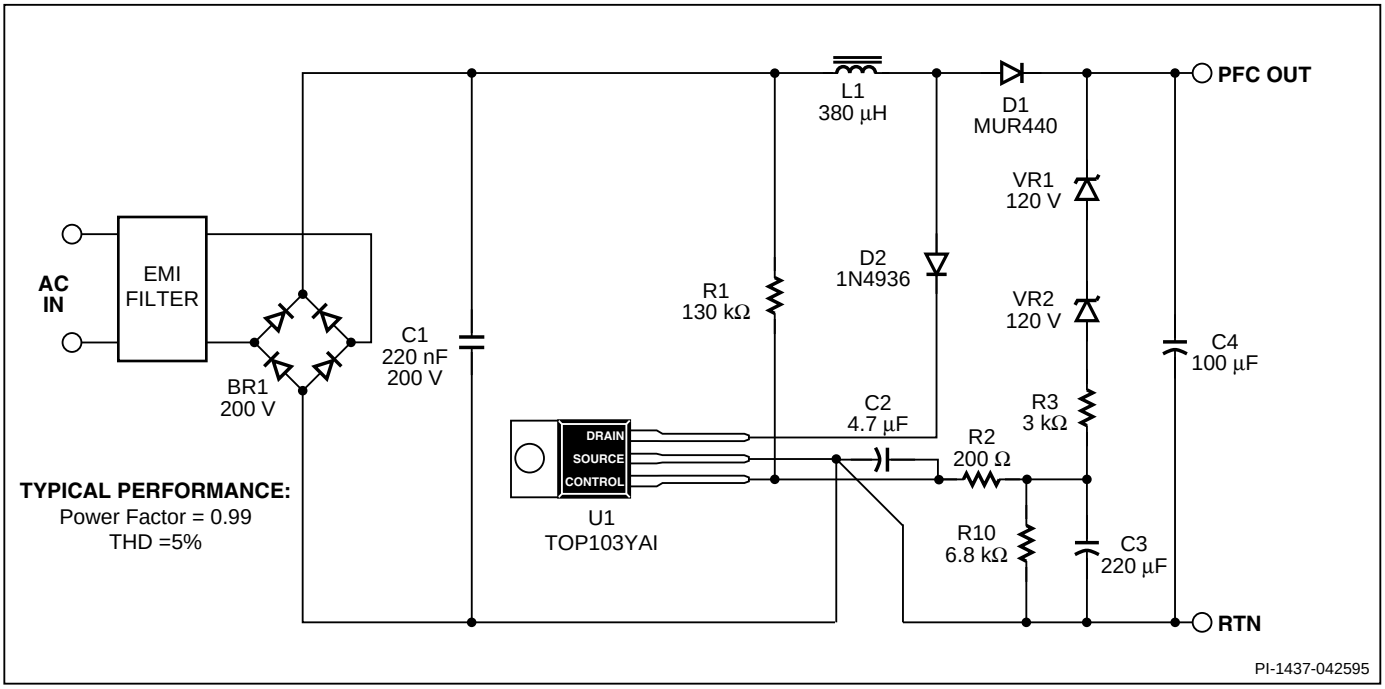


Figure 10. Schematic Diagram of a 60 W 110 VAC Input Boost Power Factor Correction Circuit Utilizing the TOP103.

General Circuit Operation (cont.)

Boost PFC Pre-regulator

TOPSwitch can also be used as a fixed frequency, discontinuous mode boost pre-regulator to improve Power Factor and reduce Total Harmonic Distortion (THD) for applications such as power supplies and electronic ballasts. The circuit shown in Figure 10 operates from 110 VAC and delivers 60 W at 265 VDC with typical Power Factor over 0.99 and THD of 5%. Bridge Rectifier BR1 full wave rectifies the AC input voltage. L1, D1, C4, and *TOPSwitch* make up the boost power stage. D2 prevents reverse current through the *TOPSwitch* body diode due to ringing voltages generated by the boost inductance and parasitic capacitance. R1 generates a pre-compensation current proportional to the instantaneous rectified AC input voltage which directly varies the duty cycle. C2 filters high frequency switching currents while having no filtering effect on the line frequency pre-compensation current. R2 decouples the pre-compensation current from the large filter capacitor C3 to prevent an averaging effect which would increase total harmonic distortion. C1 filters high frequency noise currents which could cause errors in the pre-compensation current.

When power is first applied, C3 charges to typically 5.7 volts before *TOPSwitch* starts. C3 then provides *TOPSwitch* bias current until the output voltage becomes regulated. When the output voltage becomes regulated, series connected Zener diodes VR1 and VR2 begin to conduct, drive current into the *TOPSwitch* control pin, and directly control the duty cycle. C3 together with R3 perform low pass filtering on the feedback signal to prevent output line frequency ripple voltage from varying the duty cycle. For more information, refer to Design Note DN-7.

Key Application Issues

Keep the SOURCE pin length very short. Use a Kelvin connection to the SOURCE pin for the CONTROL pin bypass capacitor. Use single point grounding techniques at the SOURCE pin as shown in Figure 11.

Minimize peak voltage and ringing on the DRAIN voltage at turn-off. Use a Zener or TVS Zener diode to clamp the DRAIN voltage.

Do not plug the *TOPSwitch* device into a “hot” IC socket during test. External CONTROL pin capacitance may deliver a surge current sufficient to trigger the shutdown latch which turns the *TOPSwitch* off.

Under some conditions, externally provided bias or supply current driven into the CONTROL pin can hold the *TOPSwitch* in one of the 8 auto-restart cycles indefinitely and prevent starting. Shorting the CONTROL pin to the SOURCE pin will reset the *TOPSwitch*. To avoid this problem when doing bench evaluations, it is recommended that the V_C power supply be turned on before the DRAIN voltage is applied.

CONTROL pin currents during auto-restart operation are much lower at low input voltages (< 20 V) which increases the auto-restart cycle period (see the I_C vs. Drain Voltage Characteristic curve).

Short interruptions of AC power may cause *TOPSwitch* to enter the 8-count auto-restart cycle before starting again. This is because the input energy storage capacitors are not completely discharged and the CONTROL pin capacitance has not discharged below the pin internal power-up reset voltage.

In some cases, minimum loading may be necessary to keep a lightly loaded or unloaded output voltage within the desired range due to the minimum ON-time.

For additional applications information regarding the *TOPSwitch* family, refer to AN-14.

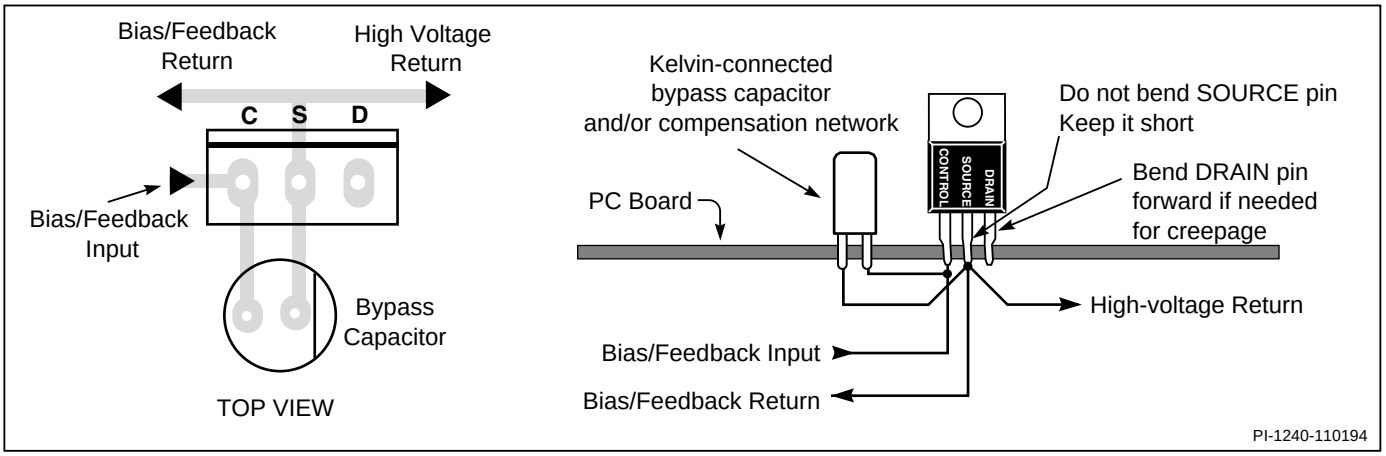


Figure 11. Recommended TOPSwitch Layout.

ABSOLUTE MAXIMUM RATINGS(1)

DRAIN Voltage ..... -0.3 to 350 V
CONTROL Voltage ..... - 0.3 V to 9 V
Storage Temperature ..... -65 to 125°C
Operating Junction Temperature(2) ..... -40 to 150°C
Lead Temperature(3) ..... 260°C
Thermal Impedance (θ_{JA}) ..... 70°C/W
Thermal Impedance (θ_{JC})(4) ..... 2 °C/W

1. Unless noted, all voltages referenced to SOURCE, T_A = 25°C.
2. Normally limited by internal circuitry.
3. 1/16" from case for 5 seconds.
4. Measured at tab closest to plastic interface.

Specification	Symbol	Conditions (Unless Otherwise Specified) See Figure 14 SOURCE = 0 V T_j = -40 to 125°C		Min	Typ	Max	Units
CONTROL FUNCTIONS							
Output Frequency	f_{OSC}	I_C = 4 mA, T_j = 25˚C		90	100	110	kHz
Maximum Duty Cycle	DC_{MAX}	$I_C = I_{CD1}$ + 0.5 mA, See Figure 12		64	67	70	%
Minimum Duty Cycle	DC_{MIN}	I_C = 10 mA, See Figure 12		1.0	1.8	3.0	%
PWM Gain		I_C = 4 mA, T_j = 25˚C See Figure 4		-11	-16	-21	%/mA
PWM Gain Temperature Drift		See Note 1			-0.05		%/mA/˚C
External Bias Current	I_B	See Figure 4		1.5	2.5	4	mA
Dynamic Impedance	Z_C	I_C = 4 mA, T_j = 25˚C See Figure 13		10	15	22	Ω
Dynamic Impedance Temperature Drift					0.18		%/˚C
SHUTDOWN/AUTO-RESTART							
CONTROL Pin Charging Current	I_C	T_j = 25˚C	V_C = 0 V	-2.4	-1.9	-1.2	mA
			V_C = 5 V	-2	-1.5	-0.8	
Charging Current Temperature Drift		See Note 1			0.4		%/˚C
Auto-restart Threshold Voltage	$V_{C(AR)}$	S1 open			5.7		V

Specification	Symbol	Conditions (Unless Otherwise Specified) See Figure 14 SOURCE = 0 V T_j = -40 to 125°C	Min	Typ	Max	Units
SHUTDOWN/AUTO-RESTART (cont.)						
UV Lockout Threshold Voltage		S1 open		4.7		V
Auto-restart Hysteresis Voltage		S1 open	0.6	1.0		V
Auto-restart Duty Cycle		S1 open		5	8	%
Auto-restart Frequency		S1 open		1.2		Hz
CIRCUIT PROTECTION						
Self-protection Current Limit	I_{LIMIT}	TOP100 di/dt = 160 mA/µs, T_j = 25˚C	0.88		1.25	A
		TOP101 di/dt = 280 mA/µs, T_j = 25˚C	1.50		2.15	
		TOP102 di/dt = 400 mA/µs, T_j = 25˚C	2.20		3.10	
		TOP103 di/dt = 520 mA/µs, T_j = 25˚C	2.85		4.00	
		TOP104 di/dt = 600 mA/µs, T_j = 25˚C	3.30		4.60	
Leading Edge Blanking Time	t_{LEB}	I_C = 4 mA		150		ns
Current Limit Delay	t_{ILD}	I_C = 4 mA		100		ns
Thermal Shutdown Temperature		I_C = 4 mA	125	145		°C
Latched Shutdown Trigger Current	I_{SD}	See Figure 13	25	45	75	mA
Power-up Reset Threshold Voltage	$V_{C(RESET)}$	S2 open	2.0	3.3	4.2	V

Specification	Symbol	Conditions (Unless Otherwise Specified) See Figure 14 SOURCE = 0 V T_j = -40 to 125°C		Min	Typ	Max	Units
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	TOP100 I_D = 110 mA	T_j = 25°C		6.4	7.5	Ω
			T_j = 100°C		10.5	12.4	
		TOP101 I_D = 190 mA	T_j = 25°C		3.6	4.3	
			T_j = 100°C		6.0	7.1	
		TOP102 I_D = 270 mA	T_j = 25°C		2.6	3.0	
			T_j = 100°C		4.2	5.0	
		TOP103 I_D = 350 mA	T_j = 25°C		2.0	2.4	
			T_j = 100°C		3.3	3.9	
		TOP104 I_D = 400 mA	T_j = 25°C		1.7	2.0	
			T_j = 100°C		2.8	3.3	
OFF-State Current	I_{DSS}	Device in Latched Shutdown I_C = 4 mA, V_{DS} = 280 V, T_A = 125°C				500	µA
Breakdown Voltage	BV_{DSS}	Device in Latched Shutdown I_C = 4 mA, I_D = 500 µA, T_A = 25°C		350			V
Rise Time	t_r	Measured With Figure 8 Schematic			100		ns
Fall Time	t_f	Measured With Figure 8 Schematic			50		ns
SUPPLY							
DRAIN Supply Voltage		See Note 2		36			V
Shunt Regulator Voltage	$V_{C(SHUNT)}$	I_C = 4 mA		5.5	5.8	6.1	V
Shunt Regulator Temperature Drift					±50		ppm/°C
CONTROL Supply/ Discharge Current	I_{CD1}	Output MOSFET Enabled		0.6	1.2	1.6	mA
	I_{CD2}	Output MOSFET Disabled		0.5	0.8	1.1	

Specification	Symbol	Conditions (Unless Otherwise Specified) See Figure 14 VS2 = 16 V R1 = 0 Ω SOURCE = 0 V T_j = -40 to 125°C		Min	Typ	Max	Units
LOW INPUT VOLTAGE OPERATION (See Note 3)							
DRAIN Supply Voltage		See Note 4		16			Volts
CONTROL Pin Charging Current		T_j = 25°C	V_C= 0 V	-2.3	-1.65	-1	mA
			V_C= 5 V	-1.2	-0.64	-0.28	mA
Auto-restart Duty Cycle		S1/Open			4	8	%
Auto-restart Frequency		S1/Open			0.85		Hz

NOTES:

1. For specifications with negative values, a negative temperature coefficient corresponds to an increase in magnitude with increasing temperature, and a positive temperature coefficient corresponds to a decrease in magnitude with increasing temperature.

2. It is possible to start up and operate *TOPSwitch* at DRAIN voltages well below 36 V. Refer to the "Low Input Voltage" Specification section for details.

3. This section specifies only parameters affected by low input voltage operation (Drain Voltages less than 36 V). All other parameters remain unchanged.

4. For low input voltage applications, the primary peak current could be set to a lower value than the current limit to increase efficiency. Refer to the Output Characteristics graph (Drain Current vs. Drain Voltage). The voltage across the transformer primary during the ON time is the difference between the input voltage and the drain voltage ($V_{DS(ON)}$).

   For example, if the input voltage is 16 VDC and a TOP104 (3.3A minimum current limit) is used at a primary peak current of 1A. Then the ($V_{DS(ON)}$) is 3 V at 100°C and the energizing voltage across the transformer primary is 13 V.

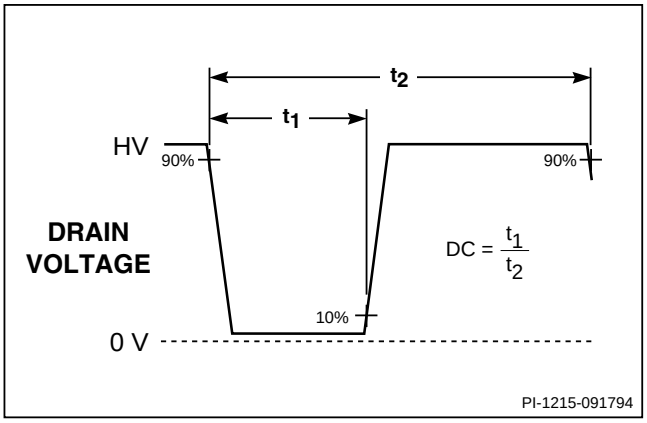


Figure 12. TOPSwitch Duty Cycle Measurement.

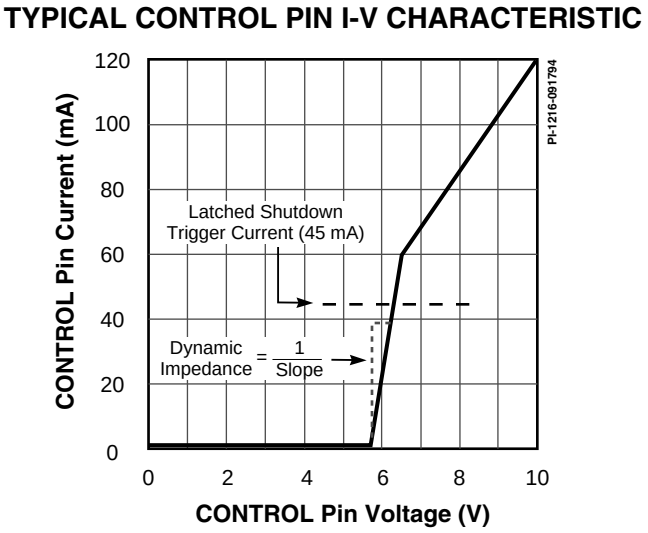


Figure 13. TOPSwitch CONTROL Pin I-V Characteristic.

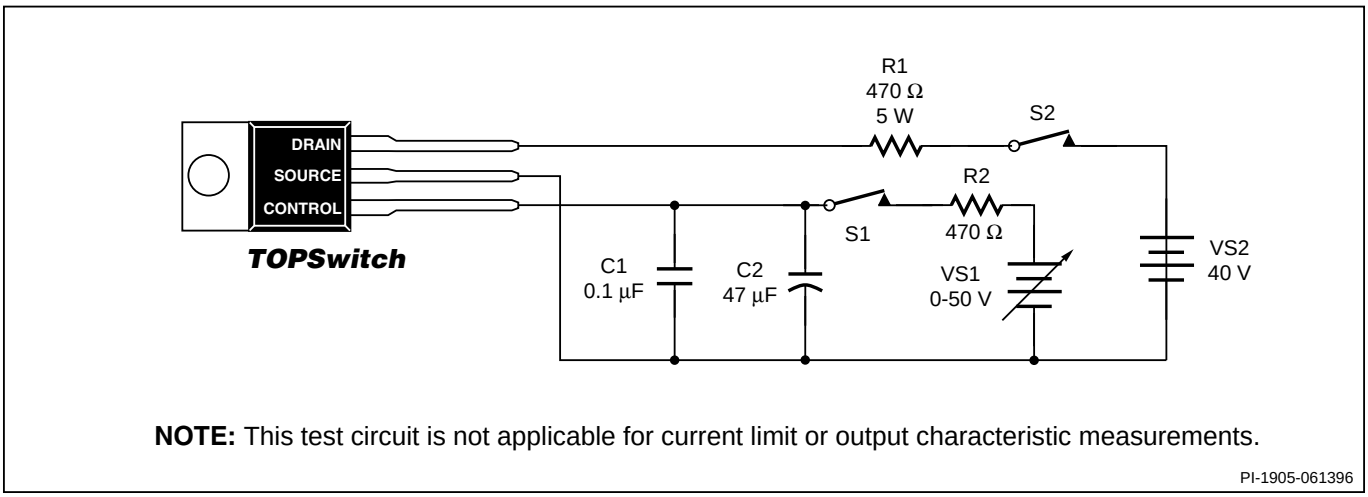


Figure 14. TOPSwitch General Test Circuit.

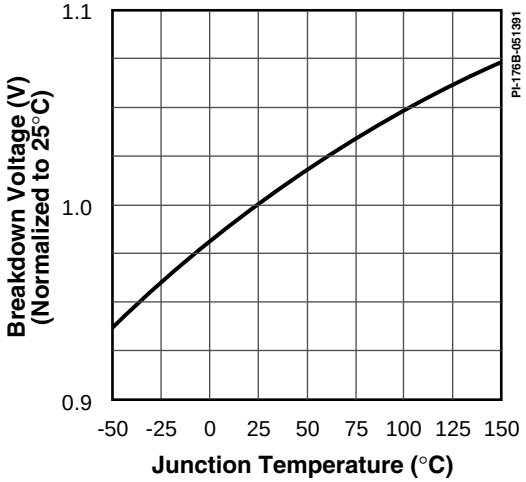
BENCH TEST PRECAUTIONS FOR EVALUATION OF ELECTRICAL CHARACTERISTICS

The following precautions should be followed when testing *TOPSwitch* by itself outside of a power supply. The schematic shown in Figure 14 is suggested for laboratory testing of *TOPSwitch*.

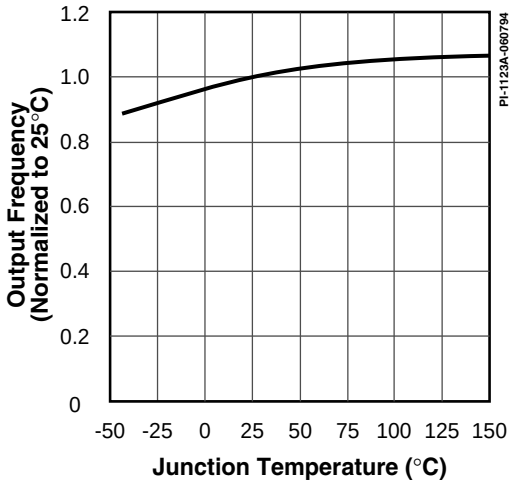
When the DRAIN supply is turned on, the part will be in the auto-restart mode. The control pin voltage will be oscillating at a low frequency from 4.7 to 5.7 V and the DRAIN is turned on every eighth cycle of the CONTROL pin oscillation. If the CONTROL pin power supply is turned on while in this auto-restart mode, there is only a 12.5% chance that the control pin oscillation will be in the correct state (DRAIN active state) so that the continuous DRAIN voltage waveform may be observed. It is recommended that the V_C power supply be turned on first and the DRAIN power supply second if continuous drain voltage waveforms are to be observed. The 12.5% chance of being in the correct state is due to the 8:1 counter.

Typical Performance Characteristics

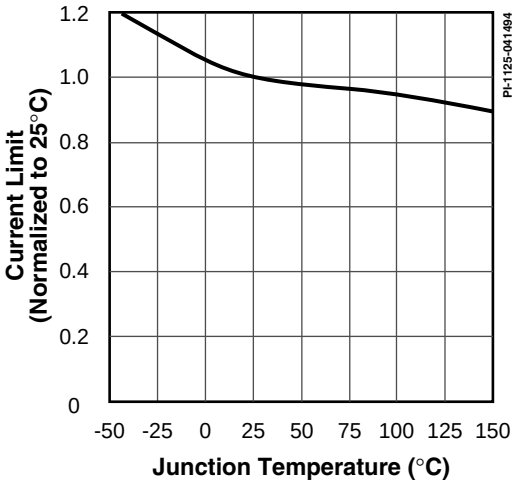
BREAKDOWN vs. TEMPERATURE



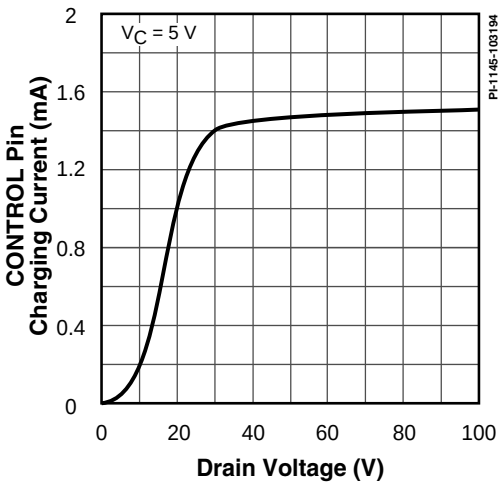
FREQUENCY vs. TEMPERATURE



CURRENT LIMIT vs. TEMPERATURE

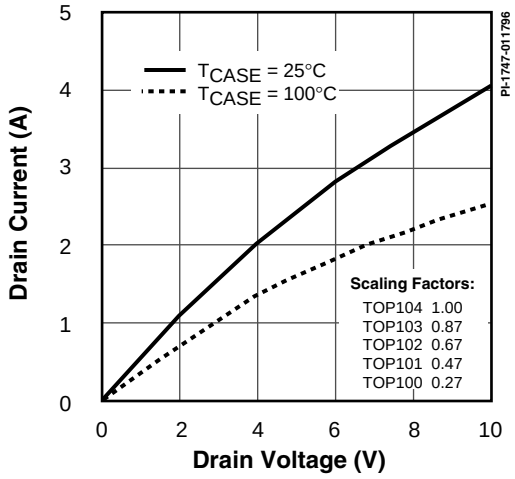


I_C vs. DRAIN VOLTAGE

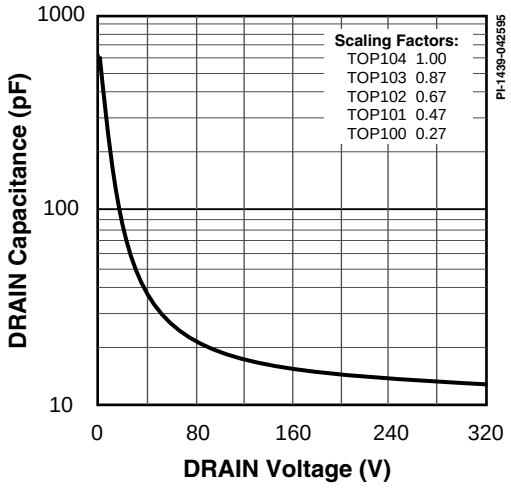


Typical Performance Characteristics (cont.)

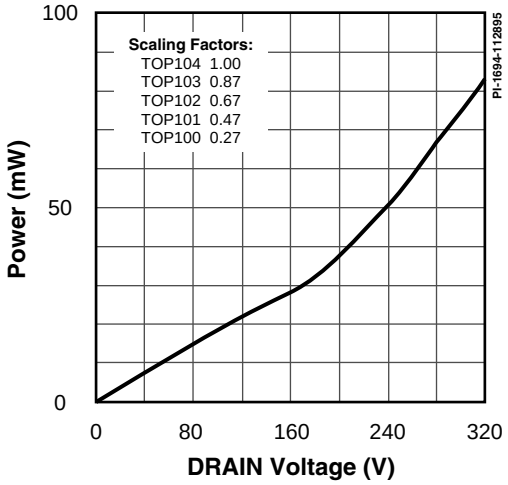
OUTPUT CHARACTERISTICS



C_{OSS} vs. DRAIN VOLTAGE



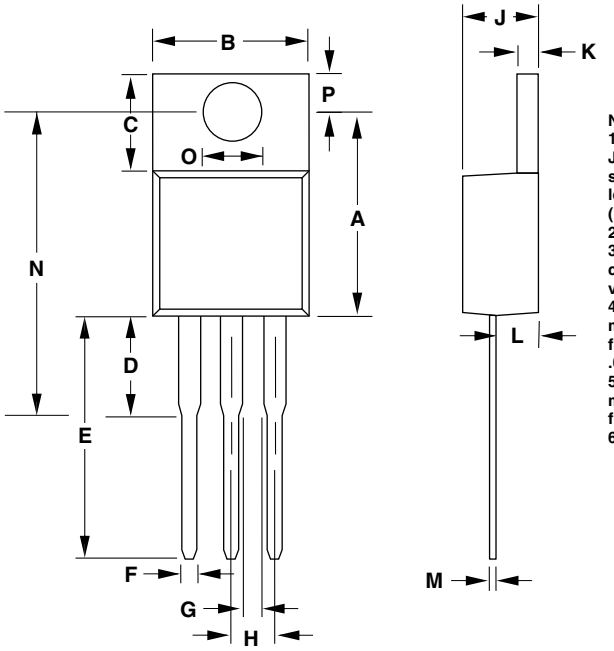
DRAIN CAPACITANCE POWER



Y03A — Plastic TO-220/3

DIM	inches	mm
A	.460-.480	11.68-12.19
B	.400-.415	10.16-10.54
C	.236-.260	5.99-6.60
D	.240 - REF.	6.10 - REF.
E	.520-.560	13.21-14.22
F	.028-.038	.71-.97
G	.045-.055	1.14-1.40
H	.090-.110	2.29-2.79
J	.165-.185	4.19-4.70
K	.045-.055	1.14-1.40
L	.095-.115	2.41-2.92
M	.015-.020	.38-.51
N	.705-.715	17.91-18.16
O	.146-.156	3.71-3.96
P	.103-.113	2.62-2.87

*** LEADS AND TAB ARE SOLDER PLATED**



Notes:
1. Package dimensions conform to JEDEC specification TO-220 AB for standard flange mounted, peripheral lead package; .100 inch lead spacing (Plastic) 3 leads (issue J, March 1987)
2. Controlling dimensions are inches.
3. Pin numbers start with Pin 1, and continue from left to right when viewed from the top.
4. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15 mm) on any side.
5. Position of terminals to be measured at a position .25 (6.35 mm) from the body.
6. All terminals are solder plated.

PI-1848-050696

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